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Quantum Confinement Effect of Ultrathin-SOI on double-gate-nMOSFETs

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Introduction: Ultrathin-SOI (UT-SOI) double gate (DG) transistors have become a focus of great interest in recent years due to the possibility of realizing deca-nano-scaled FET structures. There are many studies concerning the characteristics of SOI devices from both experimental and theoretical points of view. However, there are few reports of agreement between the results of theoretical and experimental studies concerning UT-SOI capacitor. It is important to reproduce measured characteristics with using no fitting parameters by simulation that is correctly based on the inherent physics of UT-SOI layer at the basic research stage of development. In this paper, we firstly report close agreement between measured and theoretical CV curves in ***different back-gate bias*** (V_{BG}) conditions using a one-dimensional (1D) high-precision simulator (SOI1d) that includes ***no fitting parameter***. It should be noted that SOI1d has also been used to reproduce SOI thickness (T_{SOI}) dependence of the threshold voltage (V_{TH})[1]. In addition, we describe the calculation method of SOI1d, which has not been published elsewhere.

Quantum confinement effect of UT-SOI layer: Fig. 1 shows schematically the quantum confinement effect of UT-SOI structures and the well-known surface quantization of MOS structures, assuming a single valley condition. The effect opens the same energy gaps among all the subbands since the subbands are completely confined within regions of the same width (T_{SOI}), whereas the surface quantization opens narrower gaps among higher subbands merging to the conduction band. If we use the Stern-Howard method developed for analyzing the surface quantization, then the calculated capacitance is smaller by 9% than the measured is. Therefore, in order to correctly calculate CV curve of UT-SOI, we must take into account the higher subbands, including information of valley structures (2-fold and 4-fold electrons, and light and heavy holes), and profiles of the band edges in UT-SOI.

Present calculation: Fig. 2 schemes a measured and calculated structure including UT-SOI layer, wherein there is the Z-axis perpendicular to the surface at the center of channel. SOI1d is basically a 1D Poisson-Schrödinger solver along the Z-axis from the bottom of the substrate to the top of the gate poly-Si including UT-SOI layer. So, SOI1d includes the surface quantization effect of accumulation layers and the depletion effect in the poly-Si. Fig. 3 shows the depletion effect of the poly-Si. There exists an incomplete depletion layer between the depletion layer and the bulk poly-Si, since the Fermi energy level (E_F) is higher than the conduction band edge (E_C). The incomplete depletion layer disappears in the (non-degenerate) substrate where $E_C>E_F$. Since the impurity ionization rate is decreased with the increase of carrier density [2], the ionization rate is almost the unity in the depletion layer, lower in the incomplete depletion layer, and further lower in the bulk. Since the band-gap narrowing (BGN) and the ionization rate affects each other, they are self-consistently calculated in SOI1d. Fig. 4 shows the surface quantization effect of the poly-Si accumulation layer. This effect sweeps out electrons from the poly-Si surface because the poly-Si accumulation layer is too narrow for electrons to be confined there. The increase of density-of-states is however caused by band-bending, resulting in a weak accumulation in the surface of poly-Si. The poly-Si accumulation effect might be overestimated if the surface quantization of poly-Si were neglected. These phenomena concerning poly-Si surface affects V_{TH}. The implemented Schrödinger equation involves 4 branches (2-fold and 4-fold electrons, and light and heavy holes) with 20 eigenvalues for each branch. Each eigenvalue corresponds to subband including two-dimensional momentum-space parallel to the silicon and poly-Si surfaces. Occupation rate of each subband is calculated by using Fermi-Dirac statistics. We neglect the subbands whose occupation rate is less than 0.1%, with the result that the number of subbands is at most 3. Incomplete impurity ionization and BGN [2] is also taken into account in all the silicon regions (including the substrate, UT-SOI, and poly-Si) by using Fermi-Dirac statistics. The ionization rate and BGN are significantly overestimated if the Boltzmann approximation is assumed [3]. Direct tunneling is omitted since both the buried oxide (BOX) and the front gate oxide (FOX) are so thick. The gate length is so long, as seen in Fig. 2, that 1D analysis can perform high precise calculation.

Results: Fig. 5 shows the calculation result of CV curve for DG-pMOSFET and DG-nMOSFET. It is found that the capacitance is underestimated if the quantum confinement effect is neglected in UT-SOI. Figs. 6, 7 and 8 show extremely good agreement between measured and calculated CV curves including ***back-gate bias dependence*** for T_{SOI}=3.3nm, 4.6nm and 6.4nm, respectively. It should be noted that the V_{BG} dependence is necessary to estimate T_{SOI} dependence of V_{TH} [1]. Fig. 9 shows the lowest (single peak) envelope functions of 2-fold and 4-fold branches by marks when the front gate bias (V_{FG}) is 0.5V and V_{BG}=0. Lines depict energy levels. The peaks shift to the right-hand side where the conduction band bends, in order to gain kinetic energy. Fig. 10 shows the second lowest (double peak) envelope function by lines with marks under V_{FG}=0.5V and V_{BG}=0. Lines without marks depict energy levels. The higher peak shifts to the left-hand side to loose the kinetic energy. Fig. 11 shows a similar characteristic in the triple peak envelope function under V_{FG}=0.5V and V_{BG}=0. There isn't 4-fold branch because the corresponding occupation rate is less than 0.1%. The trends described in Figs. 9-11 may affect the distribution of carrier concentration when the electric field is strong in the UT-SOI layer. Fig. 12 shows that there are double peaks in the distribution of carrier concentration in UT-SOI layer under V_{FG}=3V and V_{BG}=0. The broad peak on the left is composed of higher peaks in the double and triple peak envelope functions shown in Figs. 10 and 11. The sharp peak on the right is composed of the single peak envelope function shown in Fig. 9. The line shows that if the higher subbands are neglected, then the left peak disappears. This may result in that the center of carrier distribution (Z_{Center}) shifts to the right-hand side. Fig. 13 shows this shift on the left axis and the capacitance on the right axis when T_{SOI} is ranging from 2nm to 6nm. When T_{SOI} is greater than 4nm, both the shift and the capacitance are increased if the higher subbands are neglected. In other words, defining EOT of DG-nMOSFETs as a sum of the front gate oxide thickness (T_{FOX}) and the discrepancy between Z_{Center} and the interface with FOX, ***EOT decreases if the higher subbands are neglected.*** Fig. 14 shows T_{FOX} dependence of Z_{Center}. The upper dashed line depicts the result without the higher subbands. The lower solid line depicts the result with the higher subbands. The shift of Z_{Center} due to the neglecting of the higher subbands is suppressed by the decrease of T_{FOX}. In addition, Z_{Center} increases with the decrease of T_{FOX} since the electric field is enhanced in the UT-SOI layer if T_{FOX} is decreased.

Summary: We performed highly precise calculation of CV curve of UT-SOI DG-nMOSFETs and obtained extremely good agreement with measurement, including ***the back gate bias dependence***. It should be noteworthy to say that this agreement is achieved by using ***no fitting parameter***. In addition, we clarified the envelope functions from the lowest to higher subbands, and associated them with the distributions of carrier concentrations in UT-SOI layer. By this result, it is found that EOT is underestimated by the calculation if the higher subbands are neglected. Such an error in EOT is however suppressed by decreasing T_{SOI} and T_{FOX}.

References

[1] K. Uchida, et. al., IEDM, pp. 47-50, 2002.
[2] H. Watanabe and S. Takagi, J. Appl. Phys., **90**, 1600 (2001)
[3] H. Watanabe, SSDM, pp. 410-411, 2002.

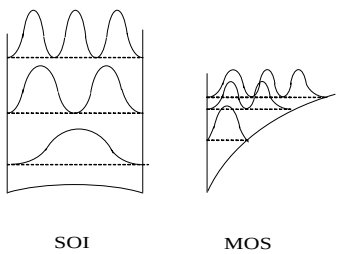

Fig. 1 Quantum confinement effect of UT-SOI and surface quantization effect of silicon surface

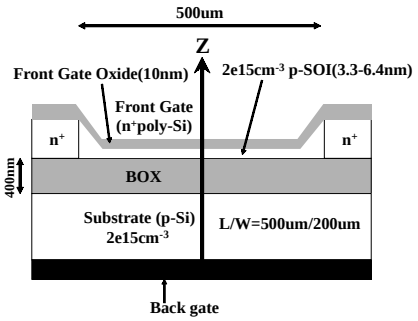

Fig. 2 A Scheme of measured and calculated structure

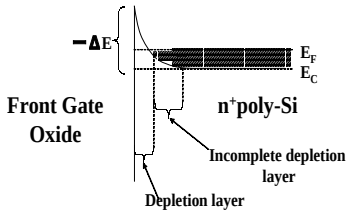

Fig. 3 A scheme of poly-Si depletion layer

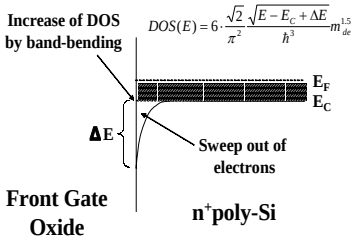

Fig. 4 A Scheme of surface quantization effect in poly-Si accumulation layer

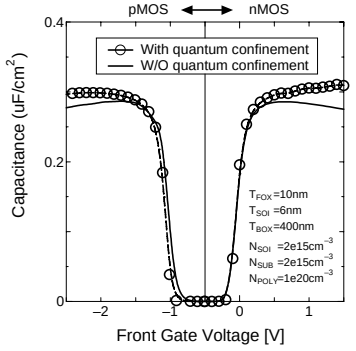

Fig. 5 Effect of quantum confinement on CV curve

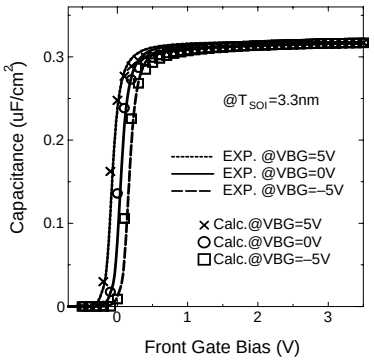

Fig. 6 Comparison of measured and calculated CV curves for T_{SOI}=3.3nm

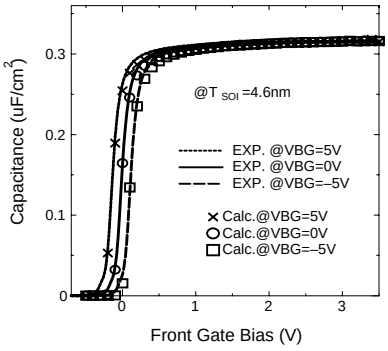

Fig. 7 Comparison of measured and calculated CV curves for T_{SOI}=4.6nm:

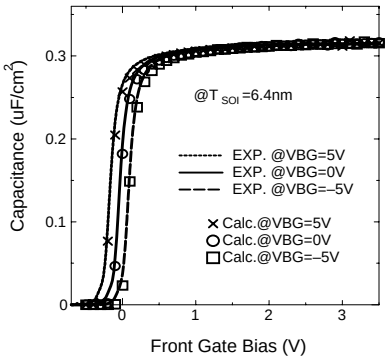

Fig. 8 Comparison of measured and calculated CV curves for T_{SOI}=6.4nm

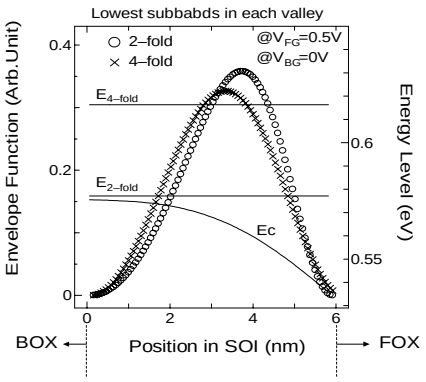

Fig. 9 The lowest envelope functions

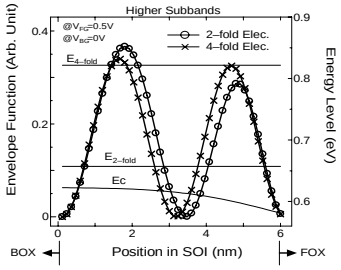

Fig. 10 Envelope functions of higher subbands

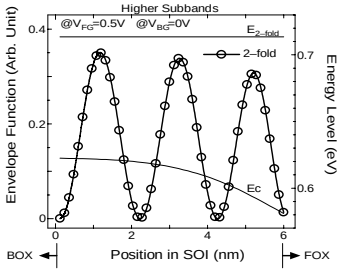

Fig. 11 Envelope function of next higher subband

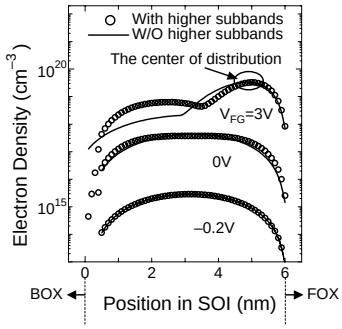

Fig. 12 V_{FG} dependence on the distribution of carrier

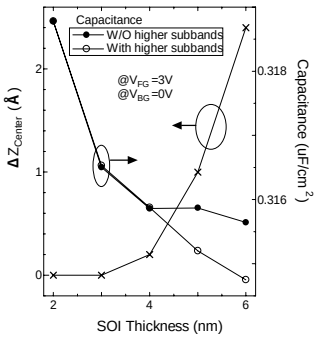

Fig. 13 Effects of higher subbands on Z_{Center} on the left axis and the capacitance on the right axis

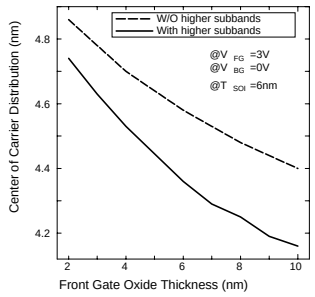

Fig. 14 T_{FOX} dependence of Z_{Center}