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Variable Body Effect Factor FD SOI MOSFET for Ultra-Low Power VTCMOS Applications

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1. Introduction

Recently, the increase in power consumption has been an emerging problem in the VLSI design, and the collaboration between device and circuit technologies is essential to reduce the power. The Variable Threshold voltage CMOS (VTCMOS) scheme [1][2] is one of the most promising circuit schemes to realize high speed and low power VLSIs. In the VTCMOS scheme, the device can attain high drive current in the active mode and low leakage current in the standby mode by changing threshold voltage (V_{th}) using the substrate bias.

Fully depleted (FD) SOI MOSFET is also a promising candidate for future VLSI. However, the application of the VTCMOS scheme to FD SOI [3][4] has had a serious problem. Due to thick buried oxide (BOX), the body effect factor γ of FD SOI is usually too small to modulate V_{th}. If BOX is very thin in order to obtain large γ, then parasitic capacitance between drain and substrate increases as well as drive current is degraded mainly due to vertical electric field.

In this paper, we propose a new device concept: variable γ FD SOI MOSFET by changing substrate depletion layer capacitance. In the active mode, the substrate just below BOX is depleted and therefore γ becomes small resulting in high drive current and small drain capacitance. In the standby mode, on the other hand, the substrate is accumulated or inverted, and γ becomes large to achieve large V_{th} shift and thus lower off-current. The validity of the proposed device concept has been confirmed by two-dimensional device simulation [5] and experiment.

2. Concept of FD SOI MOSFETs with Modulated γ

The body effect factor γ is defined in this study as [6],

$$\gamma = \left| \frac{\Delta V_{th}}{\Delta V_{bs}} \right| . \qquad (1)$$

In long channel devices, γ is determined by,

$$\gamma = \frac{C_B}{C_{ox}} \qquad (2)$$

where C_{ox} is the gate oxide capacitance and C_B is the series capacitances under the channel (series capacitance of C_{SOI}, C_{BOX}, and C_D where C_D is the substrate depletion layer capacitance). Although values of C_{SOI} and C_{BOX} are fixed, C_D can be modulated by substrate bias. In the proposed device, γ is varied by modulating C_D.

Fig. 1 shows schematics of the proposed device structure (This is an example of NMOS where the substrate is p-type.). The device has very thin BOX (~ 10 nm). In the active mode (Fig. 1(a)), slightly positive substrate voltage (V_{sub}) is applied. Then, the substrate is depleted, and γ becomes very small according to eq. (2). In the standby mode (Fig. 1(b)), negative V_{sub} is applied so that the substrate is inverted (in the case of p-type substrate) or accumulated (n-type substrate). Then, C_D can be neglected and γ becomes larger because of large C_{SOI} and C_{BOX}.

3. Simulation and Experiment

The two-dimensional simulation has been performed to confirm the advantage of the proposed device. Three types of devices are compared:
Type A: thin BOX / substrate with high N_A.
Type B: thick BOX / substrate with high N_A.
Type C (proposed): thin BOX / substrate with low N_A.
The values of BOX thickness and substrate impurity concentration N_A are summarized in Table 1. Other device parameters are fixed. Fig. 2 shows V_{sub} dependence of V_{th}. The slope of Fig. 2 corresponds to the value of γ. In Type A and B, C_D can be neglected due to very high N_A, and therefore the value of γ is almost fixed, as expected from eq. (2). Type A has very large γ due to thin BOX and Type B has small γ. In Type C, on the other hand, the value of γ suddenly changes around V_{sub} = -0.3V, because the substrate is inverted when V_{sub} < -0.3 V and depleted when V_{sub} > -0.3 V, respectively.

Fig. 3 shows $I_{off} - I_{on}$ plots in three devices when V_{sub} is varied. Although Type A has much wider range of I_{off} and I_{on} than Type B due to larger γ, Type A has smaller I_{on} at a fixed I_{off} because of large γ. Please note that Type C has very similar I_{off}-I_{on} behavior when the substrate is inverted, and it approaches to Type B when the substrate is depleted, indicating that both low leak current in the standby mode and high drive current in the active mode are achieved in Type C.

The modulation of C_D has been examined by experiments. Fig. 4 shows measured γ and S factor as a function of V_{sub} in FD SOI MOSFETs with thick buried oxide. Although the change of γ is very small due to thick buried oxide, γ is certainly varied due to the depletion of substrate.

4. Device Configuration for CMOS

Fig. 5 shows a schematic cross section of a possible CMOS device. When the substrate below NMOS is p-type, the substrate is inverted in the standby mode. Therefore, an n^+ contact that provides minority carriers in p-substrate is necessary. In this case, the substrate below PMOS should be n-type, where higher voltage than V_{dd} is applied in the standby mode and slightly lower voltage than V_{dd} is applied in the active mode. Although p-substrate for NMOS is utilized in this discussion, utilizing n-substrate for NMOS is also possible.

5. Summary

A new device concept of variable γ FD SOI MOSFET is proposed. The substrate depletion is utilized to change the body effect factor. In the active mode, the substrate is depleted and high drive current can be obtained due to small γ. Small drain capacitance is also obtained. In the standby mode, the substrate is inverted or accumulated and subthreshold current is suppressed due to large γ.

Acknowledgements

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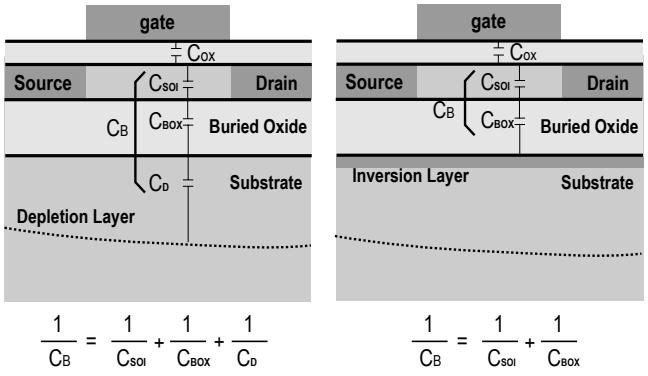

(a) Active mode (b) Standby mode

Figure 1 Schematics of proposed device structure (NMOS) with p-substrate. (a) Active mode. (b) Standby mode.

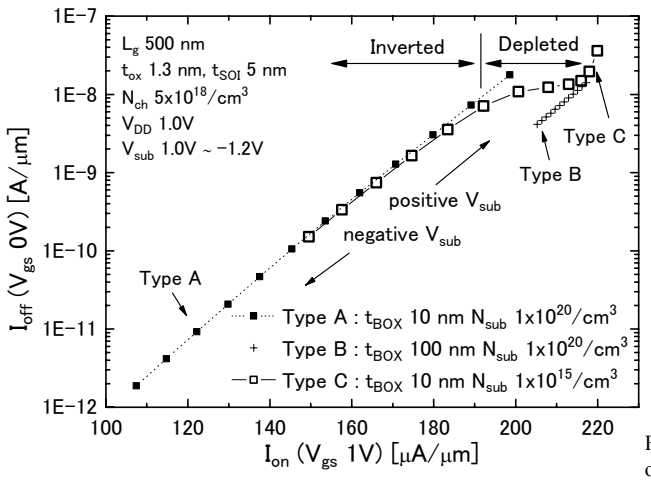

Figure 3 I_{off}-I_{on} plots in the three devices.

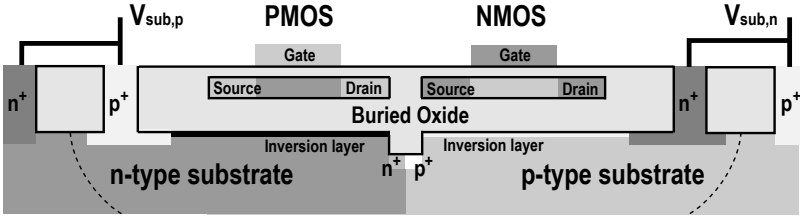

Figure 5 Schematic cross section of a possible CMOS device. N^+ contact is formed in p-substrate and p^+ contact is formed in n-substrate in order to provide carriers in the inversion layers. Careful device design will be required to connect the n^+ and p^+ contacts with the inversion layers below MOSFETs.

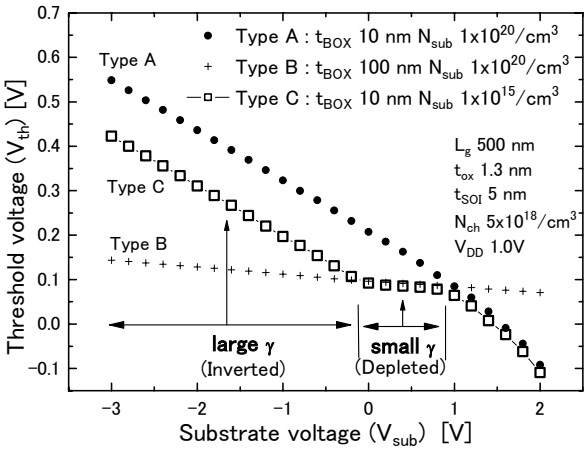

Figure 2 Simulated V_{sub} dependence of V_{th} in three types of device in Table 1. The slope of curves corresponds to the value of γ. N_{ch} is the channel impurity concentration and N_{sub} is the substrate impurity concentration.

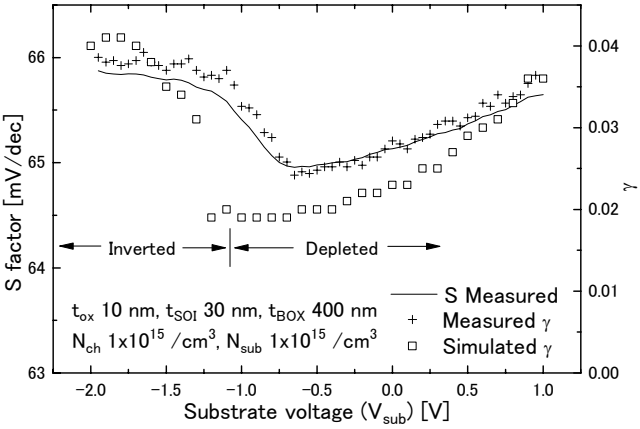

Figure 4 Measured γ and S factor of NMOS with thick t_{BOX}. The S factor of long channel devices at room temperature is expressed by $S = 60(1+\gamma)$ [6] when we consider series capacitance of C_{SOI}, C_{BOX}, and C_D. Measured γ and S factor show almost the same behaviors, indicating that the change in γ is caused by the formation of depletion layer. Simulated γ is also shown.

Table 1 Summary of device parameters used in the simulation.

	t_{BOX}	N_A
Type A	Thin (10 nm)	High ($1x10^{20}$/cm^3)
Type B	Thick (100 nm)	High ($1x10^{20}$/cm^3)
Type C	Thin (10 nm)	Low ($1x10^{15}$/cm^3)