D-4-2

Novel SOI MOSFETs with Buried Back-Gate

Hyuckjae Oh, [1]Hoon Choi, Takeshi Sakaguchi,
JeoungChill Shim, Hiroyuki Kurino, and Mitsumasa Koyanagi

Dept. of Bioengineering and Robotics , Tohoku University
01 Aza-Aoba, Aramaki, Aoba-Ku, Sendai 980-8579, Japan
Phone:+81-22-217-6909   Fax:+81-22-217-6907   E-mail: sdlab@sd.mech.tohoku.ac.jp
[1]Venture Business Laboratory, Tohoku University

1. Introduction

With the progress of portable and wireless electronic systems, high-speed devices with ultra low power consumption have become indispensable in today's ULSI application. However, conventional MOSFETs will be hard to satisfy these requirements on performance of ULSIs. Fully-depleted (FD) SOI MOSFETs have attracted noticeable attention in low-voltage high-performance applications because they have nearly ideal subthreshold slope and small parasitic capacitance.

One of the most promising ways to achieve MOSFETs with high-speed and ultra low power consumption is to vary the threshold voltage (V_{th}) of FD-SOI MOSFETs by changing back gate bias [1]. Then, we have proposed a new FD-SOI MOSFET with buried back gate which is formed by ion implantation through the SOI layer and the buried oxide into the Si substrate surface region underneath the buried oxide. Figure1 shows the proposed structure of SOI CMOSFET with buried back-gate. In this structure, the buried back gate is very effective for controlling the threshold voltage to reduce the power and enhance the performance. However, the back gate formation process may influence the device characteristics. Therefore, the back gate formation process should be carefully optimized in terms of impurity type and impurity concentration in the SOI layer and the back gate region. In this paper, back gate formation technology and electrical characteristics of fabricated FD-SOI NMOSFETs with buried back gate were studied.

2. Experiment

The fully-depleted (FD) SOI NMOSFETs with buried back-gate were fabricated with SIMOX SOI wafers (p-type, 20Ω-cm, t_{Si}/t_{BOX} = 60nm/100nm). First, the SOI layer was thinned down to ~30nm by thermal oxidation. After that, the mesa-isolation for active region formation was carried out. Then, phosphorus was implanted and annealed for the back-gate formation. The condition of implantation and annealing was 150keV in energy, 5×10^{13}cm^{-2} for dosage and 1000^0C, 30min in Ar atmosphere, respectively. BF$_2$ implantation (20keV, 7×10^{12}/cm^2) was performed for channel doping to adjust the threshold voltage. Next, 2.5nm thick gate oxide (SiO$_2$) was thermally grown at 800^0C. After the poly-Si gate electrode patterning, one mono layer of arsenic atoms was adsorbed for the source and drain extension (SDE) formation using atomic layer doping (ALD) technology. Silicon selective epitaxial growth (SEG) process was carried out on S/D region for elevated S/D formation followed by gate sidewall formation. After deep S/D regions were formed, Ni salicidation process with the multi-step annealing method was applied to the gate and S/D regions [2]. Finally, contact holes and Al wirings were formed to complete FD-SOI NMOSFETs with buried back-gate. Cross-sectional SEM images of fabricated FD-SOI MOSFET are shown in Fig. 2(a). Figure 2(b) shows SEM image of buried back-gate region. It is clear from the figure that FD-SOI NMOSFET with buried back-gate is successfully fabricated.

3. Results and Discussion

To verify the optimally tailored buried back-gate formation condition for CMOS applications, the influences of impurity type and impurity concentration not only in the back gate region of the substrate but also in the SOI layer on the device characteristics such as V_{th} value, SCE and mobility have to be carefully investigated. In order to form the buried back gate, the ion implantation through the SOI layer and the buried oxide was carried out. Therefore, if a significant amount of impurity atoms remain in the SOI layer, the threshold voltage changes seriously. The, we measured the impurity profiles in the SOI layer and the back gate region by SIMS. Figure 3 shows SIMS profiles of boron (a) and phosphorus (b) implanted through the SOI layer and the buried oxide as a function of annealing condition. As is obvious in the figure, boron and phosphorus concentrations in the SOI layer are considerably reduced to below 1×10^{16}/cm^3 and to the order of 10^{16}/cm^3, respectively by introducing the furnace annealing (1000^0C, 30min in Ar). It is believed that these impurity concentrations in SOI layer might be low enough to minimize the influences on electrical characteristics of SOI MOSFETs. Meanwhile, the back gate impurity concentrations at the substrate surface underneath the buried oxide are in order of 10^{19}/cm^3 for boron and in order of 10^{20}/cm^3 for phosphorus, respectively.

In order to evaluate the dependence of phosphorus concentration on the SOI layer thickness, the simulation was performed using T-SUPREM4 simulator. As shown in the Fig.4, the phosphorus concentration in the SOI layer significantly decreases as the SOI layer thickness is reduced while the back gate phosphorus concentration at the substrate surface hardly changes. Therefore, we can exclude the influences of phosphorus remained in the SOI layer by employing thin SOI layer.

In this work, FD-SOI NMOSFETs with phosphorus buried back gate are vigorously investigated. Figure 5 shows subthreshold characteristics of SOI NMOSFET with the gate length of 0.15μm as a function of back gate bias. As shown in the figure, the threshold voltage is shifted to the positive voltage direction by applying the negative back gate bias voltage. It was confirmed from the figure that the back gate is very effective not only for decreasing off-current but also for controlling the threshold voltage. The back gate is also effective for increasing the immunity to the short channel effect (SCE). Figure 6 shows I_D-V_D characteristics as a function of back gate bias. The back gate effects of devices with relatively longer gate length of 0.25 μ m were investigated in order to evaluate the back gate effect excluding the SCE. Measured and simulated subthreshold characteristics and transconductances (g_m) of SOI NMOSFET with the gate length of 0.25 μ m are shown in Fig. 7 and Fig.8 (a), respectively. Both characteristics indicate that the threshold voltage is remarkably changed by changing the back gate bias voltage. Specifically, the threshold voltage is significantly shifted to the negative voltage direction when the large positive back gate bias voltage is applied. This is due to the formation of back

channel at the interface between the SOI layer and the buried oxide. Fig. 8 (b) shows the simulated subthreshold characteristics and transconductances (g_m) of SOI NMOSFET with the thinner buried oxide of 50nm. As is clear from the figure, the threshold voltage can be more effectively controlled by the back gate as the buried oxide thickness is reduced. The threshold voltage is plotted as a function of back gate bias voltage in Fig.9. It is obvious again from this figure that the back gate is very effective to control the threshold voltage and to reduce the off-currents.

4. Conclusions

We proposed a new SOI MOSFET with buried back gate. It was confirmed by the experiment and the simulation that the back gate is very effective for controlling the threshold voltage and to reduce the off-current.

References

[1] T. Hiramoto, et. al., *IEICE Trans. Electron*, vol.E83-C,No.2, Feb. 2000.

[2] J.C.Shim et. al., *2002 SSDM Tech. Dig.*,pp.434 , 2002
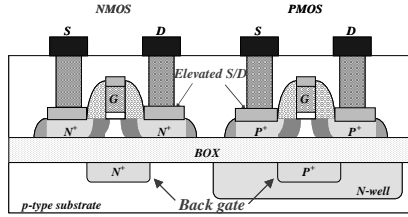
Fig. 1 Cross-sectional structure of FD-SOI MOSFETs
with buried back gate

(a) SEM image of SOI MOSFET (b) SEM image of buried back-gate

Fig.2 Cross-sectional SEM image of SOI MOSFET
with buried back-gate
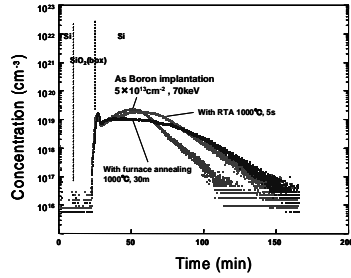
(a) Boron profiles
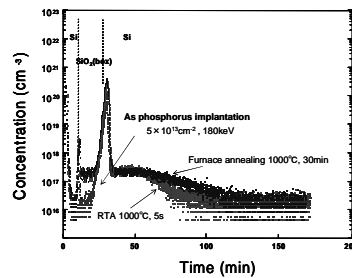
(b) Phosphorus profiles

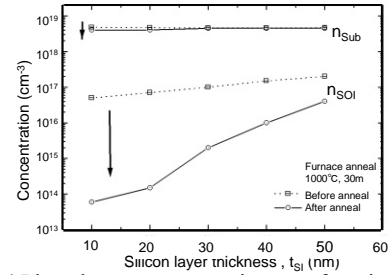Fig. 3 SIMS profiles of implated SOI wafer for buried back-gate formation

Fig.4 Phosphorus concentration as a function
of SOI layer thickness (simulation results)
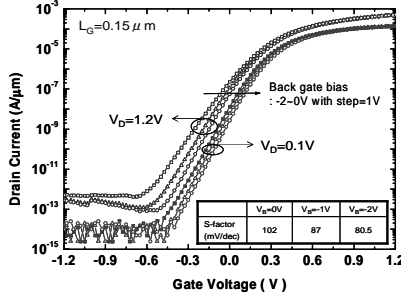
Fig. 5 Measured subthreshold characteristics
as a function a function of back-gate bias
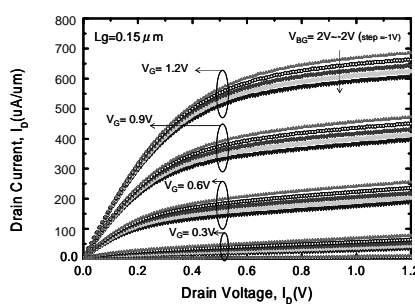
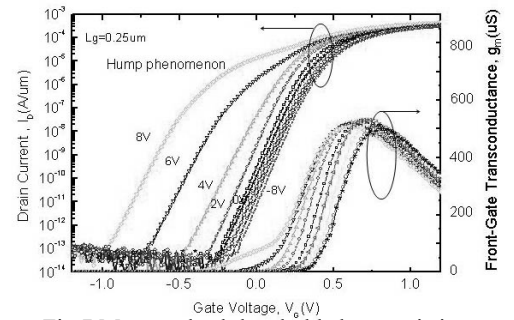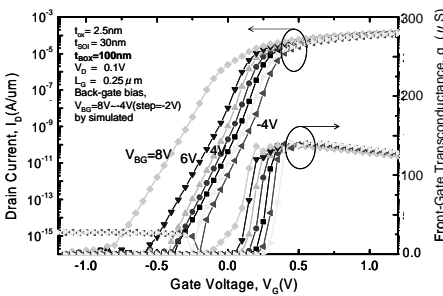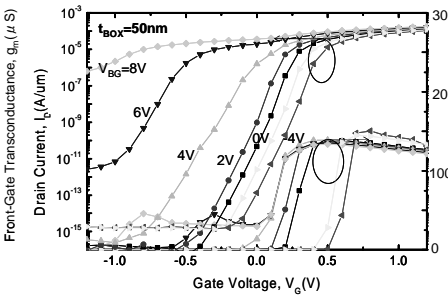Fig. 6 Measured I_D-V_D characteristics
as a function of back-gate bias

Fig.7 Measured subthreshold characteristics
of back gate bias (V_{BG}=8V~-8V)

(a) Buried oxide thickness t_{BOX}=100nm

(b) Buried oxide thickness t_{BOX}=50nm

Fig. 8 Simulated subthreshold characteristics as a function
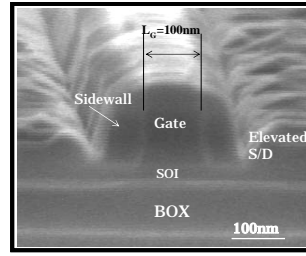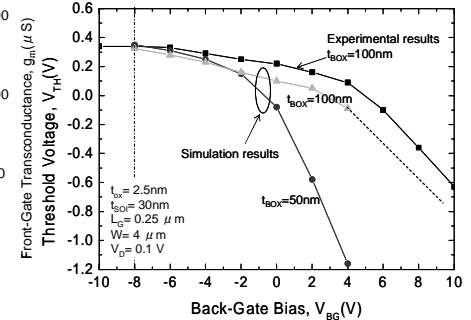back gate bias (V_{BG}=8V~-4V)

Fig. 9 Threshold voltage as a function of of
back gate bias