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Modeling of Fully-depleted SOI Device Variation

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1. Introduction

In scaled-down LSI, the trade-off relationship between process margin and circuit performance becomes more serious. Conventionally, worst-case analysis is widely used to calculate process margin. To realize good performance and high yield LSI in short time, accurate device statistical models are required in early stages of the development. Some groups have proposed TCAD-based approaches and these approaches give good prediction of device variations.

Fully-depleted (FD) SOI MOSFET has advantages in short channel effects and subthreshold characteristics [1]. On the other hand, FD-SOI characteristics fluctuate easily by SOI thickness (Tsi) variation [2]. To realize good performance and high yield FD-SOI devices, we have to predict device fluctuation accurately including Tsi effects. This is the first problem tackled by this work. Furthermore, it is not clear whether such prediction can be applied to worst-case analysis in which correlation of nMOSFETs and pMOSFETs is important. This is the second problem of this work. The aim of this work is to clarify these two problems through the comparison of TCAD predictions to manufactured distributions.

2. Method

To give good TCAD prediction, it is important to adjust the model parameters to experiment data [3]. Typical simulation results by using the calibrated model are compared to fabrication data in Fig.1. Calibrated TCAD models agree well with dependence of threshold voltage on Tsi and gate length (Lg). Overall errors of these models are below 0.03 volts. The model accuracy is sufficient to be used in further statistical analysis.

It should be mentioned here that cross-term sensitivity of Tsi and Lg is the key point of this calibration. Because short channel effects of FD-SOI depend strongly on Tsi.

3. Results

(1) Device variation analysis

In order to confirm the validity of TCAD model applied to σTsi effects, simulations are compared with fabrication data. First, a number of TCAD simulations are performed according to design of experiments (DoE) taking process condition as parameters [4]. Next, response surface functions (RSF's) of Vth and Ids are extracted from simulation results. Monte Carlo method is applied to these RSF's and results are compared to statistical distributions of fabrication data. For both short (Fig.2) and long (Fig.3) channel devices, TCAD /RSF's results agree well with fabrication data.

Fig.4 shows comparison of σTsi-σVth between long channel and short channel. It is noteworthy that variation of long channel characteristics is larger than short channel's. When Tsi changes 10nm, Vth changes 0.03V for short channel devices and 0.05V for long channel devices. In long channel devices, Tsi affects positively to Vth's. But in short channel devices, Tsi affects negatively because of short channel effect. Thus, long channel devices have more serious problem concerning Tsi variation.

For the prediction of short channel devices, the cross-term effects of Tsi and Lg on Vth are important. In the case of Fig.2, cross-term effects are as large as 25% of Lg variation effects.

(2) Correlation between nMOSFET and pMOSFET device characteristics

Process variations are considered in circuit design by worst-case models or recently by statistical model [5]. Typical worst-case models are represented by correlation of nMOS and pMOS saturation current (Idsat). Fig.5 and Fig.6 show scatter plots of Ids of nMOSFETs (Idn) and pMOSFETs (Idp) obtained from fabrication data (Fig.5) and from RSF's (Fig.6). In this case, we compared long channel devices, because short channel devices are affected by gate length's variation. With including σTsi, RSF's results agree well with fabrication data. As σTsi becomes large, not only σIdn and σIdp but also correlation factors of them become large. This is because Tsi of nMOSFETs and pMOSFETs in a chip are almost equal. Thus, TCAD approach predicts the correlation factors of nMOSFETs and pMOSFETs accurately considering Tsi effects.

4. Conclusions

We present FD-SOI devices variation analysis by the TCAD/RSF approach.

1) TCAD approaches are useful for the early prediction of FD-SOI variations. The key point for this approach is to care the accuracy for cross-term effects of Tsi and Lg.

2) For the effects of σTsi to device fluctuations are more serious in long channel device. In short channel devices, a part of Tsi effects is canceled by short channel effects.

3) The correlation factors of nMOSFETs and pMOSFETs become larger when σTsi is large. This is also an important point for circuit design of FD-SOI's. Sufficient accuracy of statistical model is obtained by the TCAD/RSF approach considering σTsi.

As one of the novel devices, FinFET is proposed. Fig.7 shows FinFET simulation results using Selete 3-D process/device simulator ENEXSS [6]. When Fin height (Tsi) changes 5nm, Vth changes about 0.07V. The influence of FinFET of Tsi is larger than FD-SOI. For FinFET design, since Tsi control becomes still more important, it is thought that the importance of this approach increases.

Acknowledgements

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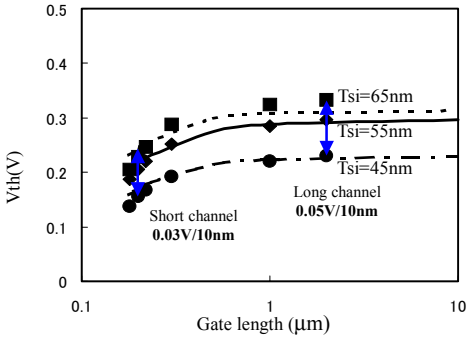

Fig.1 Vth-Lgate comparison between calibrated model (lines) and fabrication data (dots)

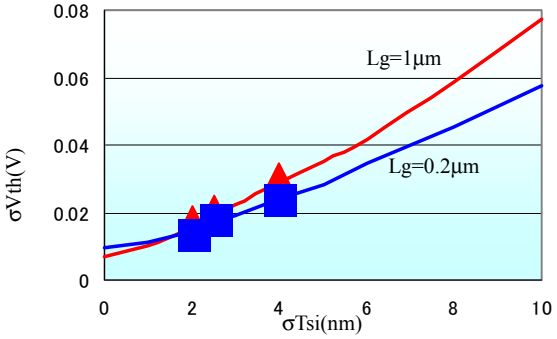

Fig.4 Comparison of σTsi-σVth between long channel and short channel

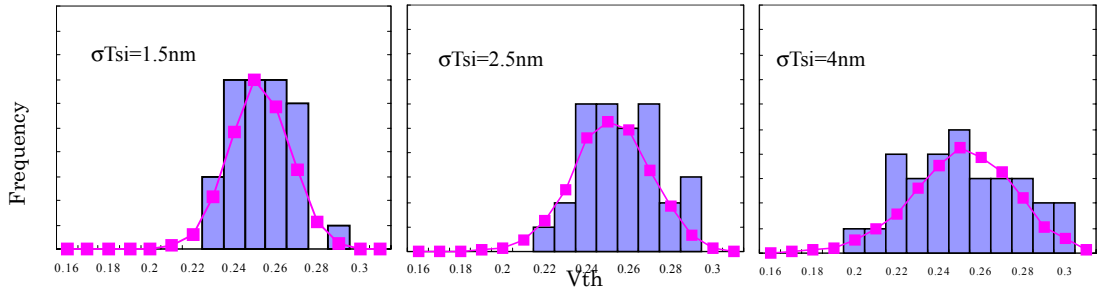

Fig.2 Measured histograms of Vth. TCAD results (lines with marks) agree well with experimental data (poles)

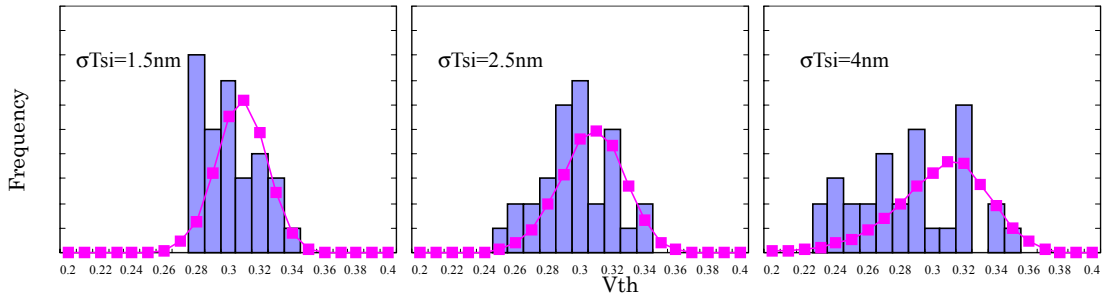

Fig.3 Measured histograms of Vth (Lg=1.0um)

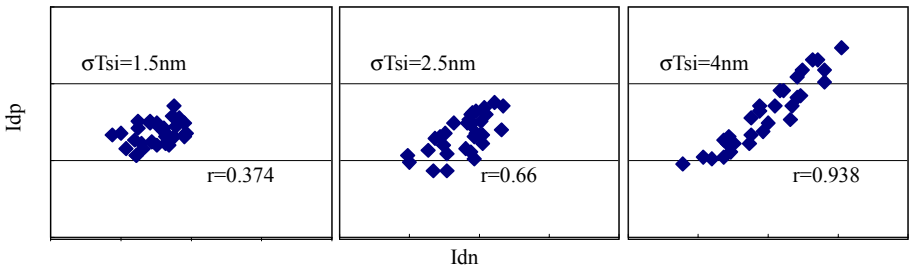

Fig.5 Scatter plots of Ids of nMOSFETs (Idn) and pMOSFETs (Idp) obtained from fabrication data

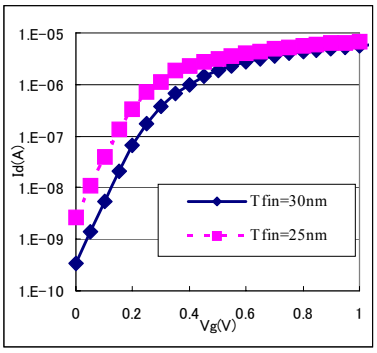

Fig.7 FinFET Id-Vg simulation results (Vd=0.05V)

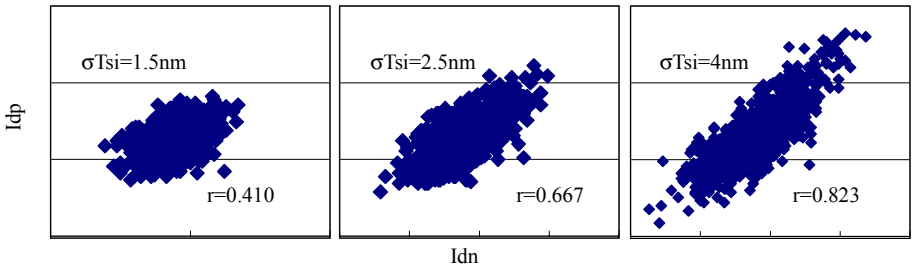

Fig.6 Scatter plots of Vth of nMOSFETs (Vtn) and pMOSFETs (Vtp) obtained from RSF's