Temperature Dependence of Threshold Voltage and Hot Carrier Degradation of Dynamic Threshold SOI-pMOSFETs

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Introduction

Dynamic threshold MOSFETs (DT-MOSFETs), proposed by Assaderaghi et al. [1], were attractive for low power supply applications. The threshold voltage operating under DT mode is reduced due to the forward biasing of the body, so the current drive can be significantly improved under the on state. Since the device exhibits the same normal-mode $V_{TH}$ in the off state (because $V_{gs}=0$), low standby power is maintained. In addition, subthreshold slope and short channel effects are also improved due to the dynamic substrate bias. Further, by applying DT-mode operation to partially depleted silicon-on-insulator (PD-SOI) MOSFETs, the junction leakage current can be significantly reduced. In this study, we report the threshold voltage shift and hot carrier degradation on SOI pMOSFETs at different temperatures operating under both normal and DT modes.

Device Fabrication

PMOSFETs were fabricated on p-type SOI wafers and the top Si thickness was 200 nm. As\textsuperscript{+} implant with an energy of 100 keV and a dose of 1x10\textsuperscript{13} cm\textsuperscript{-2} was used for threshold voltage ($V_{TH}$) adjustment. Gate oxide thickness of 3.4 nm was grown in N\textsubscript{2}O ambient, followed by a 200nm poly-Si deposition. After S/D implantation, wafers were annealed by RTA at 1020°C for 20 sec. A 550nm TEOS oxide layer was then deposited and etched to form contact holes. Finally, a Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned. Hot carrier stressings were performed at temperatures ranging from room temperature to 100°C.

Results and Discussion

Figure 1a shows the electrical connection under DTMOS operation, where gate and body are tied together. Fig. 1b, and 1c depict device layout for H-gated and T-gated structures, respectively. Fig. 2 shows $V_{TH}$ degradations for SOI pMOSFETs at different temperatures, operating under different modes for Hgated structures. All devices were stressed at $V_{G}=V_{TH}$ and $V_{B}=-4.5V$[2]. It can be seen that the normal-mode device at room temperature depicts the worst $V_{TH}$ shift ($\Delta V_{TH}$) among all splits. Electron trapping appears to be the dominant degradation mechanism at the initial stage of stressing (i.e., before 1000 sec). After 1000-sec., $\Delta V_{TH}$ becomes negative for all devices, an indication of dominant positive charge trapping. The magnitude of $\Delta V_{TH}$ for H-gated devices in DT-mode is small (within 4mV), and is almost independent of operation temperature. In contrast, $\Delta V_{TH}$ under normal mode is inversely proportional to temperature, i.e., a higher temperature leads to a smaller $\Delta V_{TH}$. Fig. 3 shows the comparison of time dependence of $G_{mmax}$ degradation for H-gated structures. The H-gated device at room temperature under DT mode actually depicts aggravated linear $G_{mmax}$ degradation. Fig. 4 shows $G_{m}$ for SOI pMOSFETs at normal mode with different substrate biases and also under DT-mode for H-gated devices. $G_{m}$ under DT-mode is enhanced by about 60%, due to the combined effects of dynamic threshold voltage and the reduced vertical electric field (i.e., as a result of tying the gate and substrate), which helps improve the mobility. During hot-carrier stressing, the carrier mobility decreases, and the magnitude of $G_{m}$ degradation is aggravated due to the dynamic threshold voltage. However, the degradation of the devices under DT mode at high temperature stress (i.e., 75°C and 100°C) is alleviated due to a larger decrease of maximum lateral electric field $|E_L|$ at elevated temperature [3]. As shown in Fig. 5, the reduction ratio of $|V_{TH}|$ at high temperature with respect to the room temperature $|V_{TH}|$ is larger under DT-mode than normal-mode. A larger decrease in $|V_{TH}|$ with increasing temperature would result in an increase in $|V_{DSAT}|$, and therefore a decrease in $|V_{m}|$. The smaller $|V_{m}|$ results in reduced impact ionization and in turn reduced $\frac{1}{2} |V_{TH}|$ and transconductance degradation under stressing at elevated temperature. Similar results are also depicted in Fig. 6 for the degradation of $I_D$. Despite an initial increase due to electron trapping, the magnitude of $I_D$ starts to decrease due to hole trapping at longer stressing time, and is especially severe for DT-mode under room temp. Fig. 7 shows the comparison of time dependence of $G_{mmax}$ degradation for SOI pMOSFETs for T-gated devices. The transconductance degradation under DT mode at room temperature still shows the worst behavior, and improves at elevated temperature due to reduced $|E_L|$. It is worth noting that the T-gated structure depicts larger degradations than the H-gated counterparts when operating under DT-mode. This is due to the non-uniform potential distribution as a result of the single-sided body contacts for the T-gated structure under DT-mode. Fig. 8 depicts the degradation of $I_D$ for SOI pMOSFETs under different modes at different temperatures ($V_{TH}=V_{G}=-0.7V$) for T-gated structure. It shows similar, albeit worse, trend to the H-gated structure. In conclusion, we have reported the temperature dependence of $V_{TH}$ and hot carrier degradation of SOI DT-pMOSFETs. We found that the DT-mode devices depict aggravated transconductance degradation, albeit smaller $V_{TH}$ shift, compared to normal-mode SOI-pMOSFETs, and the degradations decrease at elevated temperature.

References

Fig. 1 (a) Connections of SOI MOSFETs under DT mode, (b) H-gate structure, (c) T-gate structure

Fig. 2 Stress time dependence of $V_{TH}$ degradation for H-gated SOI-pMOSFETs operating under different modes and temperatures.

Fig. 3 Linear transconductance ($V_D=-0.1V$) versus stressing time for 0.8µm H-gated devices operating under different modes and temperatures. Devices were stressed at $V_G=V_{TH}$, and $V_D=-4.5V$.

Fig. 4 Gate voltage versus transconductance for H-gated SOI-pMOSFET operating under normal mode with different substrate biases, and also under DT-mode.

Fig. 5 Ratio of threshold voltage reduction versus gate length for H-gated devices operating under different modes and temperatures.

Fig. 6 Stress time dependence of on current ($V_G=-0.7V$, $V_D=-0.7V$) degradation for H-gated SOI-pMOSFETs under different modes and temperatures. All devices were stressed at $V_G=V_{TH}$, $V_D=-4.5V$.

Fig. 7 Linear transconductance ($V_D=-0.1V$) versus stressing time for 0.8µm T-gated devices. All devices were stressed at $V_G=V_{TH}$, and $V_D=-4.5V$.

Fig. 8 Stress time dependence of on current ($V_G=-0.7V$, $V_D=-0.7V$) degradation for T-gated SOI-pMOSFETs. All devices were stressed at $V_G=V_{TH}$, $V_D=-4.5V$. 