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FinFET Promise and Challenges

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1. Introduction

The quasi-planar FinFET (Fig. 1) offers the superior scalability of a double-gate MOSFET structure together with a process flow and layout similar to that of the conventional MOSFET [1]. Hence, it recently has been investigated by several groups [2]-[4]. CMOS FinFETs with gate lengths down to 10 nm have already been demonstrated, and exhibit excellent control of short-channel effects [5].

Fig. 2 compares the performance of single-gate ultra-thin-body (SG-UTB) and double-gate (DG) SOI CMOS technologies against that of bulk-Si CMOS technology, obtained through mixed-mode simulation using realistic device structures based on ITRS specifications [6]. The use of a lightly doped or undoped channel provides immunity to variations in threshold voltage (V_T) resulting from statistical dopant fluctuations, as well as enhanced carrier mobility for higher transistor drive current because of the lower average transverse electric field in the inversion layer [7]. V_T adjustment can be achieved without channel doping, by using a tunable-work-function metal gate technology [8,9]. From Fig. 2, it is seen that the DG MOSFET used in conjunction with a suitable metal gate technology (to provide the desired V_T values without the need for channel doping) provides superior performance.

Although the FinFET is promising for scaling CMOS into the sub-10nm regime, it poses technological challenges for fully realizing the circuit-performance benefits of the DG MOSFET structure. This paper discusses some of these issues for optimizing CMOS FinFET circuit performance.

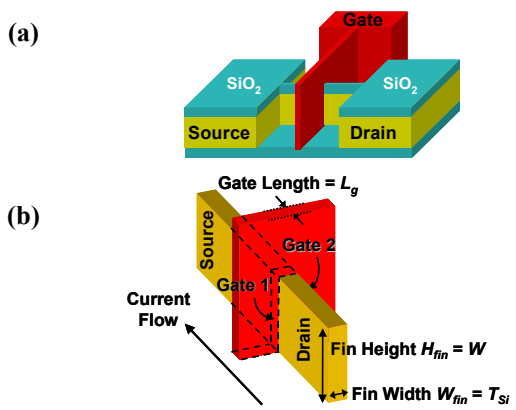


Fig. 1: (a) Quasi-planar FinFET structure. A SiO_2 hard mask is used to protect the top of the SOI film during the long gate-etch process. (b) Close-up of FinFET with key parameters labeled. (The SiO_2 hard mask is not shown here, for simplicity.)

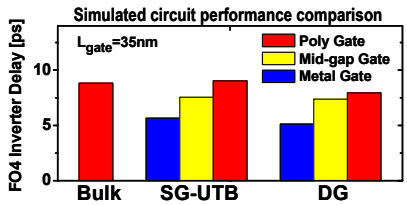


Fig. 2: Comparison of loaded-inverter (fanout=4) delay for thin-body SOI CMOS technologies against that for bulk-Si CMOS technology. For the cases of poly-Si gate (n+ poly-Si for NMOS, and p+ poly-Si for PMOS) and midgap-work-function gate, heavy channel doping is used to achieve the proper values of V_T [10].

2. FinFET Technology Challenges

Narrow Fin Formation

Generally, the minimum gate length (L_g) in an integrated circuit is the smallest feature that can be defined by conventional lithographic processes. In order to suppress short-channel effects, the thickness of a lightly doped FinFET body (*i.e.* the fin width W_{fin}) must be ~1.5× smaller than L_g, however [11]. Sub-lithographic fins (narrower than any feature that can be defined by conventional lithography) can be formed in an SOI film by using spacers, formed along the sidewalls of a sacrificial patterned layer, as a hard mask [12]. The spacers are formed by conformal deposition of the spacer material, followed by anisotropic etch to remove this material from the lateral surfaces on the wafer (Fig. 3). The width of the spacers is determined by the thickness of the deposited spacer layer, and can be very uniform across a wafer. Another advantage of the spacer lithography process is that it provides for a doubling of fin density.

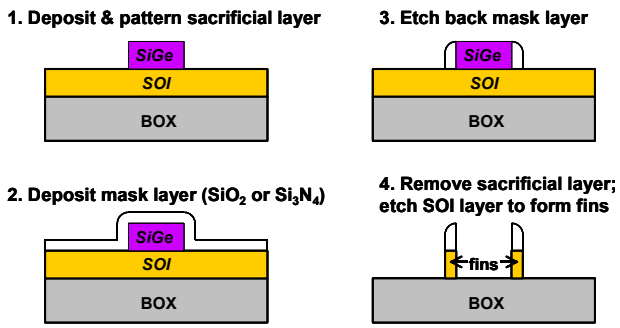


Fig. 3: Sequence of schematic cross-sections illustrating the process for forming sub-lithographic fins using sidewall spacers. Note that the fin pitch achieved is smaller by a factor of ~2 as compared with the pitch of the sacrificial layer.

Optimization of Fin Surface Orientation

The transconductance of a FinFET is dependent on its layout orientation, due to carrier mobility anisotropy in crystalline Si [3]. The channel surfaces of a FinFET lie in the (110) plane when the fin is oriented parallel or perpendicular to the wafer flat or notch of a standard (100) wafer. Hole mobility is enhanced, while electron mobility is degraded, for a (110) Si surface as compared with a (100) Si surface [13]. To simultaneously achieve maximum NMOS and PMOS drive currents, a (100) sidewall surface for NMOS and (110) sidewall surface for PMOS is desirable. This can be achieved in several ways, for example by orienting the PMOS fins to be perpendicular or parallel to the flat or notch of a (100) wafer and orienting the NMOS fins to be rotated at a 45° angle (Fig. 4).

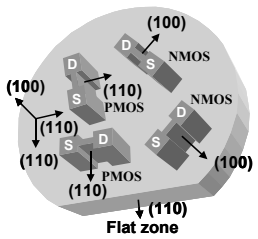


Fig. 4: Si fin orientation for optimal CMOS FinFET performance. PMOS devices have <110> fin surfaces, while NMOS devices have <100> surfaces.

Source/Drain Formation

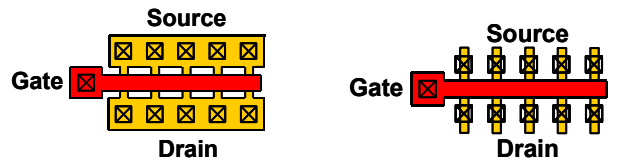
In order to minimize short-channel effects, the spacing between the source and drain (S/D) junctions should be uniform from the top of the fin to the bottom of the fin (*i.e.*, the electrical channel length L_{eff} should be uniform along the width of the channel). Ideally, then, the S/D dopants should be introduced at a 90°C angle into the sidewalls of the fin. Since multiple fins are required to achieve a wide-channel FinFET, tilted ion implantation is limited to angles <60° to avoid shadowing, assuming that the fin pitch P is at the limit of lithography ($P = 4\times L_{gmin}$). Doping techniques such as solid-source diffusion and plasma-immersion ion implantation [14] may ultimately be required to achieve perfectly uniform L_{eff} throughout the height of the fin for optimal performance.

Circuit Design Flexibility

As shown in Fig. 1b, the Si fin height (H_{fin}) is effectively the channel width. FinFETs of various effective channel widths can be practically achieved by using multiple fins in parallel [15], but with variations limited to increments of H_{fin}. Assuming that the fin aspect ratio (H_{fin}:W_{fin}) is limited to 3 (dictated by the capabilities of the Si dry-etch process used to form the fin), $H_{fin} = 3\times W_{fin} = 2\times L_{gmin}$, where L_{gmin} is the minimum gate length. If a more conservative definition for the effective channel width is used ($W_{eff} = 2\times H_{fin}$), then W_{eff} is limited to an integer number of $4\times L_{gmin}$ increments.

Parasitic Capacitance

Parasitic capacitance adversely affects circuit performance, and it becomes more significant as L_g is scaled down [16]. The parasitic gate-sidewall capacitance of a FinFET can be an issue if aggressive design rules are used for device layout (Fig. 4a). The development of a borderless fin contact process, which eliminates the need to flare out the active-area pattern in the S/D contact regions (Fig. 4b), can mitigate this issue.



(a) (b)

Fig. 5: FinFET layouts (a) for a conventional contact process, and (b) for a borderless contact process.

5. Conclusion

The FinFET is a manufacturable DG-MOSFET structure which offers superior control of short-channel effects and higher drive current as compared to the classic bulk-Si MOSFET structure. Its circuit performance benefit is maximized when a lightly doped channel is used in conjunction with a tunable-work-function gate technology for V_T adjustment. Practical (but not insurmountable) technological challenges remain to be addressed before the circuit-performance benefits of the DG-MOSFET structure can be fully realized with a CMOS FinFET technology.

Acknowledgements

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