High-Aspect Ratio Gate Formation of Beam-Channel MOS Transistor with Impurity-Enhanced Oxidation of Silicon Gate

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1. Introduction

In order to overcome scaling limit of planar MOS FET, three dimensional (3-D) transistors such as DELTA [1] and fin FET [2] have recently been proposed. Although the target of this study is to realize 3-D vertical-wall-channel transistor[3], realization of ultra-high drive current per planar area is a prime concern. Therefore, high aspect ratio of beam height $H_b$ to gate length $L_g$, $A_{H/L}$, and high beam are inevitable.

Previously $A_{H/L}$ of about 0.5 has been realized using TMAH (tetra methyl ammonium hydroxide) anisotropic etchant with 1-$\mu$m $H_b$ and 2-$\mu$m $L_g$[4]. While, an $A_{H/L}$ of the finFET is 2.5 with 50-nm $H_b$ and 20-nm $L_g$[2]. In this study, a beam-channel transistor (BCT), as shown in Fig. 1, having $A_{H/L}$ of 5 with 1-$\mu$m $H_b$ and 0.2-$\mu$m $L_g$ has been successfully realized utilizing novel gate formation technique.

One of the most difficult techniques to fabricate tall beam transistor is to realize narrow gate surrounding the tall beam. In addition, sidewall spacer sticking to the sidewall of the gate of planar MOS FET is almost impossible to be delineated by conventional RIE for the tall silicon beam. In response to the requirement, impurity-enhanced oxidation (IEO)[5] is utilized to realize the sidewall spacer. The IEO selectively forms much thicker oxide, i. e. its own oxide of polysilicon gate, which play a role of the sidewall spacer.

2. Device Fabrication

A fundamental process sequence for BCT is illustrated in Fig. 2. After beam formation on an SOI wafer with a 1.0-$\mu$m-thick SOI and a 1.5-$\mu$m-thick BOX-SiO2, a heavily doped poly-Si gate is delineated by an isotropic plasma etching to prevent polysilicon residue remains at the sidewall of the beam. The minimum beam width of 40 nm has been obtained. Then, a side-wall-spacer of SiO2 of the gate is formed by low temperature wet oxidation for 60 min at 700$^\circ$C. Utilizing this IEO, 100-nm- and 10-nm-thick oxides are formed on the gate and the SOI substrate, respectively.

Then, source and drain are formed by POCl3 gaseous doping. Finally, aluminum electrode is deposited by sputtering so that the electrode wraps sidewalls of source and drain. SEM micrographs are shown in Fig. 3.

Fig. 1 A bird’s eye view of typical beam-channel transistor.

Fig. 2 Process sequence for beam and gate formations.

(a) Polysilicon gate wrapped by its own oxide.
(b) SOI beam surrounded by polysilicon gate and CVD SiO2.

Fig. 3 Cross-sectional SEM photographs for obtained beam and gate structures.
3. Device Characteristics

The $I_{d-V_g}$ subthreshold characteristics for n-MOS transistors is shown in Fig. 4. Sufficiently small off-current is obtained. A factor of $I_{doff}T_{ox}/W_{eff}$ is about 0.035 $\mu$A $\mu$m for this BCT, while it is about 0.012 for finFET[2]. It is not yet clarified why the discrepancy occurs.

Beam width dependence of drain off-current $I_{doff}$ is shown in Fig. 5. The beam width $W_b$ measures that of top portion of the beam as previously shown in Fig. 3. It is observed that $I_{doff}$ decreases as $W_b$ becomes shorter. In particular, when $W_b$ is smaller than 300 nm, the $I_{doff}$ sharply decreases. It is speculated that this sharp cut-off occurs when both-side junctions across the beam are combined each other.

On the other hands, the beam width dependence of the drain on-current, as shown in Fig. 6, may imply that parasitic series resistances of source and drain affect the drain current resulting in the decrease in the current. This estimation is supported by experimental results shown in Fig. 7. This figure shows that rapid increase in series resistance at less than beam width of 300 nm. This means gate-to-contact spacing should be kept narrower as shown in Fig. 8. As the results it is observed, as shown in Fig. 9, substantial field-effect mobility decreases due to the parasitic resistance of narrow source and drain.

4. Conclusion

A novel gate formation technique is proposed to realize 3-D beam-channel transistor (BCT) with beam height of around 1.0 $\mu$m. BCT successfully works at minimum beam width of 40 nm and effective channel length of 200 nm.

Despite satisfactory performance of BCT, it is observed that the parasitic series resistance of source and drain formed in narrow beam adversely affects drivability of BCT. The effective structure, such as self-aligned silicidation and/or elevated source and drain, to reduce the resistance will increasingly important towards more scaling of 3-D beam channel transistor in near future.

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