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P-channel Vertical Double-Gate MOSFET Fabrication by Ion-Bombardment-Retarded Etching

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1. Introduction

Double-gate (DG) MOSFETs offer great potential in terms of their scalability in nanoscale CMOS technology [1][2]. Among DG MOSFET family, a vertical type has attracted much attention due to its controllability of channel length independently of lithography and its suitability with bulk Si substrates [3,4]. The critical issue is fabrication technology for the ultra-thin vertical channel ensuring DG MOSFET performance.

Recently, we discovered a unique phenomenon that an as-implanted Si substrate is barely etched by a hot TMAH solution which is known as an anisotropic etchant of Si [5]. This newly-discovered process, that is, ion-bombardment -retarded etching (IBRE), can successfully be applied to fabrication of an ultra-thin vertical channel beyond the lithographic limit on a bulk Si substrate. By using the IBRE, actually, we succeeded in fabricating the n-channel vertical DG MOSFET (named "IMOSFET" from its resemblance to the letter "I") with a 15-nm-thick vertical channel [6]. In this paper, we report p-channel IMOSFETs fabricated by using the same IBRE, demonstrating the suitability of the IMOSFETs as a future double-gate CMOS technology.

2. Ion-Bombardment-Retarded Etching (IBRE)

It is well known that the hot TMAH solution etches a Si substrate anisotropically. The etch rate of Si(110) surfaces is significantly higher than that of Si(111). We found that an as-implanted Si substrate is hardly etched independently of the surface orientation. As shown in Fig. 1, the etch rate of a Si(110) substrate in TMAH is markedly decreased at a dose over $3x10^{13}$ cm^{-2} for both As and BF_2 implantation. This phenomenon (IBRE) arises from the suppression of the electrochemical reaction between the Si substrate and TMAH solution as a result of the surface amorphization by ion irradiation. Thus, the IBRE is not affected by ion species at all, as can be seen in Fig. 1. This nature is favorable to form both p- and n-channel MOSFETs. By utilizing the IBRE, we can easily form an etch-stopper in/on Si substrates against the hot TMAH.

3. IMOSFET Fabrication by IBRE

The process flow of the IMOSFET is simple as summarized in Fig. 2. We used a p-type Si(110) wafer with high resistivity of 15 Ωcm for both p- and n-IMOSFETs. Both the wet etching for a thicker vertical channel (VC) formation and thinning of the VC by the IBRE were performed in 2.38% TMAH at 50˚C. 30 keV BF_2 ions were used for the VC thinning and S/D formation for p-IMOSFETs, while 30 keV As ions for n-IMOSFETs. Thinning of VC for the vertical channel of IMOSFETs was performed by the IBRE as depicted in Fig. 3. First, keV ions are perpendicularly implanted onto the thicker VC. As a result, ion implantation damages appear only at the top and bottom regions of the VC, while the side walls remain unexposed. Then the sample is dipped in the hot TMAH solution, where the damaged top and bottom regions of the VC act as etch-stoppers, and the unexposed side walls are horizontally etched by TMAH. The top and bottom regions of the VC, turn into the drain and source automatically after the following oxidation process. Next, 5-nm-thick gate oxide is grown on the (111)-oriented side walls. In-situ P-doped poly-Si is deposited conformally and etched-back by RIE to form double side gates. After TEOS-CVD SiO_2 deposition, contact holes are opened self-aligned to the top of the VC. The height and length of the fabricated VC were 160 nm and 24 μm, respectively.

4. Device Results

Cross-sectional SEM images of the VCs formed by the BF_2 IBRE and As IBRE are shown in Fig. 4. It should be noted that the VC thickness T_c is to be less than 25 nm for both cases. Since no channel engineering was employed, the channel type is estimated to be p-type for p-IMOSFETs and n-type for n-IMOSFETs by the simulation [7] as shown in Fig. 5. It is obvious from Fig. 6 that short channel effects, e.g. V_{th} lowering, DIBL and increase of s-slope, are dramatically improved for both the p- and n-IMOSFETs with decreasing T_c from 35 to 25 nm. These experimental results precisely demonstrate the unique nature of the DG MOSFET structure. In addition, relatively good current drive is achieved thanks to double channels, even for the case of a thick gate oxide of 5 nm. Further improvement in the current drive can be attained by gate oxide thinning, optimization of dopant profile, and series resistance reduction by salicidation. The inadequate threshold voltage for both the p- and n-IMOSFETs due to the n^+-poly Si gate can be adjusted by taking advantage of asymmetric n^+-p^+-poly Si gate structure [8].

5. Summary

We experimentally demonstrated that the IBRE technology enables us to easily fabricate high performance p-channel vertical DG MOSFETs (p-IMOSFETs) on a bulk Si substrate.

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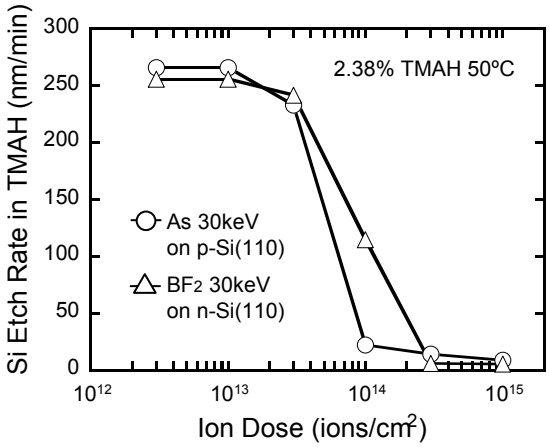

Fig. 1. Dependence of the Si etch rate (ER) in TMAH on ion dose. As the ion dose increases, the ER of Si is markedly reduced, independent of ion species and substrate conduction type.

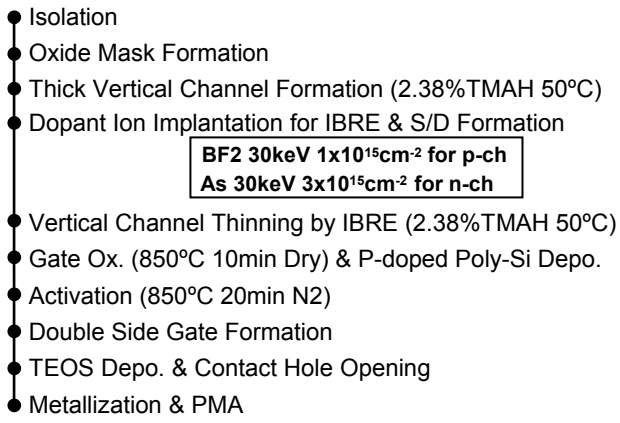

Fig. 2. Fabrication process flow of IMOSFETs. The processes are the same for p- and n-IMOSFETs, except the dopant ion implantation species.

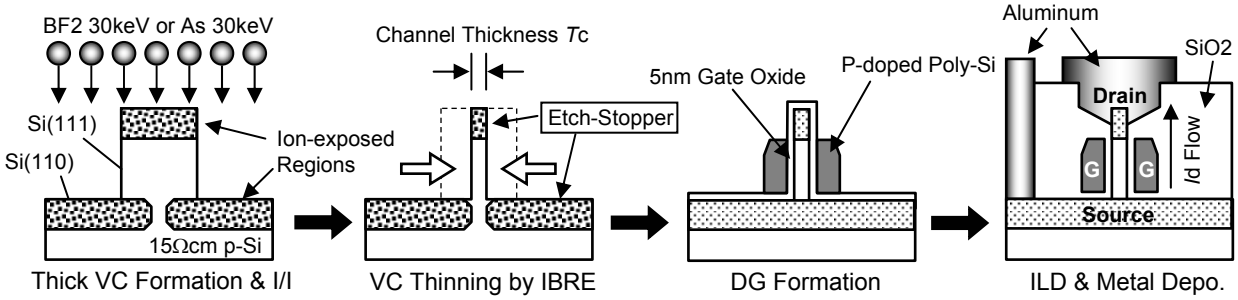

Fig. 3. Schematic fabrication process flow of p- and n-IMOSFETs.

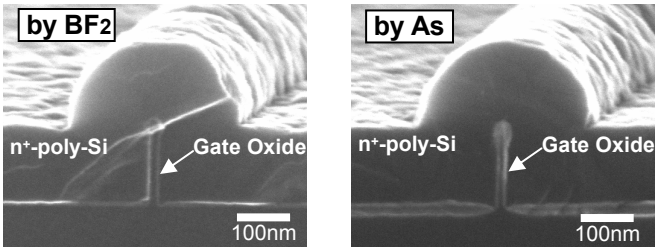

Fig. 4. Cross-sectional SEM pictures for the ultra-thin vertical channels formed by utilizing BF2 or As IBRE.

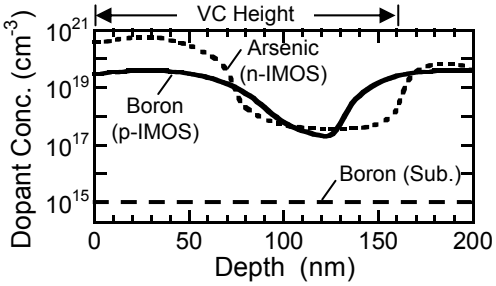

Fig. 5. Simulated dopant profile in the vertical channels for the p- and n-IMOSFET.

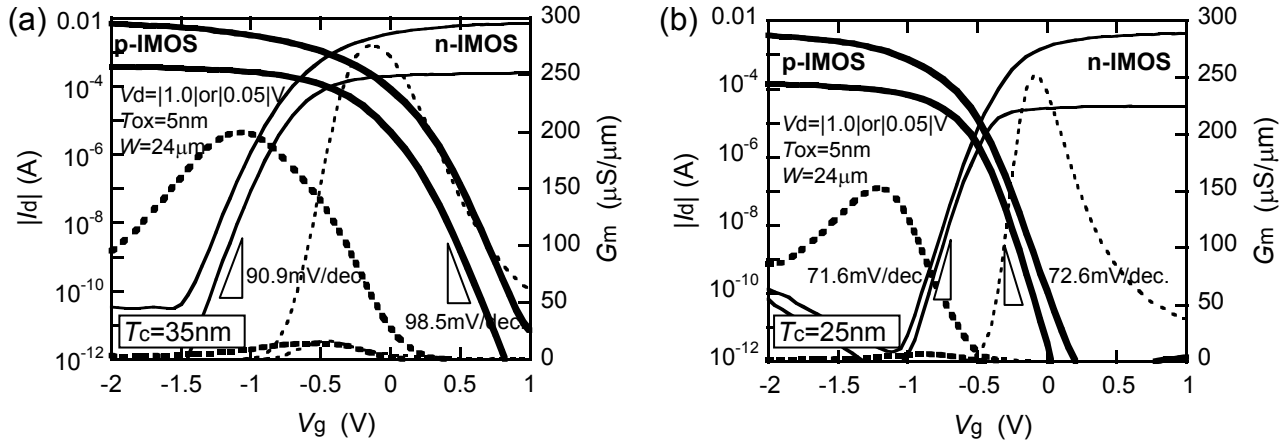

Fig. 6. *I*d-*V*g (solid line) and *G*m-*V*g (dotted line) plots of the fabricated p-IMOSFETs (thick line) and n-IMOSFETs (thin line) with (a) *T*c=35nm, and (b) *T*c=25nm. As the channel thickness *T*c decreases, the SCEs, such as *V*th lowering, DIBL and increase of s-slope, are successfully improved for both the p- and n-IMOSFET.