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SiGe in Advanced CMOS Devices – - an unique material equally helpful when present or absent

Thomas Skotnicki

STMicroelectronics, Crolles, France
850, rue Jean Monnet, 38926 Crolles, France
Phone: +33 (0)4 76 92 68 29 E-mail: thomas.skotnicki@st.com

1. Introduction

The first MOSFETs were built on Germanium that were next replaced by Silicon. It is amazing that these two former opponents are now becoming "good friends" collaborating within SiGe alloys that find the more and more applications in modern CMOS technologies.

It is well known that SiGe in the gate reduces polydepletion, whereas in the channel, it leads to increased mobility. SiGe may also play a passive role like in "virtual substrates", where a thick SiGe layer only serves for creation of a mechanical strain in the active Si-layer. In some very novel applications (SON, Silicon-On-Nothing), SiGe is used as a sacrificial material that is removed after having transferred lattice continuity between two Si-layers.

2. SiGe PMOSFETs

Strained SiGe layers on Si-substrates have been extensively studied for boosting PMOSFET current drivability [**1-10**]. Hole mobilities obtained with these devices can be very much improved comparing with Silicon, Fig. 1, thus leading to an equivalent current increase in long devices. This increase, however, disappears gradually when shortening the gates. As analysed in [**9**], this is due to degraded subthreshold slope (buried-channel operation) that implies higher Vth to keep constant Ioff, but also due to proximity of defected areas resulting from partial SiGe relaxation caused by extension implants. Even with very reduced Si-cap thickness, the buried SiGe-channnel leads to a relaxation of the electrostatic integrity of the device, worsening the subthreshold slope, SCE and DIBL.

A clear improvement has been demonstrated [10] when replacing the single Si/SiGe layer by a double or even triple sandwich, Fig. 2. Not only the subthreshold behaviour Fig. 3, but also junction leakage (3 decades lower diode leakage) and mobility have been cured.

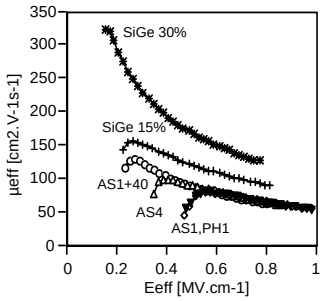


Fig. 1.

Fig. 1. Mobility enhancement in SiGe channel PMOFETs, [8].
Fig. 2. Triple Si/SiGe sandwich shows increased robustness, [10].
Fig. 3. Improved subthreshold behaviour with multiple Si/SiGe sandwich, 10].

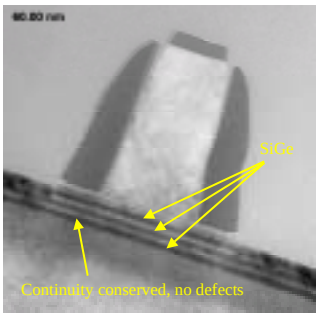


Fig. 2.

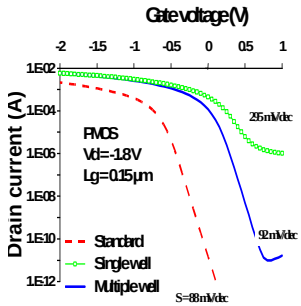


Fig. 3.

3. Strained-Si channel MOSFETs.

Tensile strain in Silicon produces increased mobility of both electrons and holes, [11]. To produce this kind of strained-Si channels, thick SiGe layers are grown by epitaxy on Silicon, leading to a rupture of lattice continuity between Si and SiGe that produces an almost perfect mono-crystal with the lattice constant corresponding to relaxed SiGe. Growing a thin Silicon layer on top of this relaxed SiGe thus leads to tensile strain in the Silicon layer, Fig. 4. Enhancement of electron mobility in this kind of strained-Si layers has been confirmed in many papers, e.g. [12-17]. Even at strong effective fields the gain may be as large as 80%, Fig. 5. The remaining issues relevant to this architecture reside in poor heat dissipation of the virtual substrates, and in higher strain needed for holes than for electrons in order to produce the same gain in mobility.

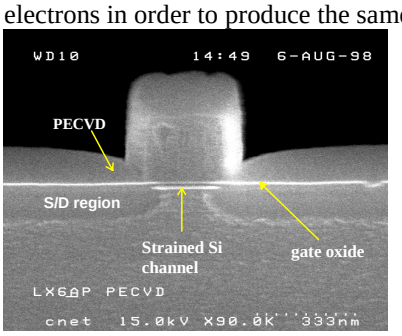
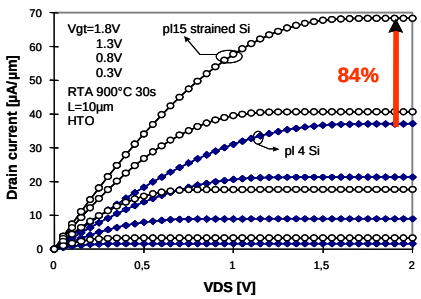


Fig. 4. SEM photo of a MOS transistor with strained Si channel, from [16].

Fig. 5. Strained-Si channel MOSFET and its output characteristics, data from [16].



4. Notched gates

SiGe can also be very useful as gate material allowing not only reduced gate poly-depletion, [18-19], but also etching notched, [20], or ultimately short gates with sub-lithographic feature resolution, [21]. This latter technique led us to demonstrate one of the shortest operational planar devices (16nm gate length), Fig. 6. This 16nm transistor has received a very special design to enhance punchthrough via the non-overlapped regions (low doping). Thanks to that, the non-overlap regions do not present large series resistances as it would be the case with the conventional design. Consequently, not only the overlap capacitance was cancelled but also well-behaved characteristics Fig. 7 were obtained. In spite of Ion current being slightly lower than in overlapped structure, the gain in Cgate has prevailed (total cancellation of the overlap), and the CV/I for this device is well placed on the same tendency-line as for the best overlapped transistors, Fig. 8.

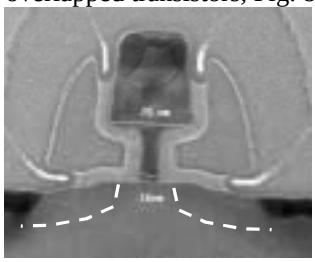


Fig. 6.

Fig. 6. TEM cross-section of the 16nm MOS, from [21].
Fig. 7. Id(Vd) curves measured on the 16nm NMOSFET, data from [21].
Fig. 8. CV/I measured on the 16nm ST transistor in comparison with data from literature.

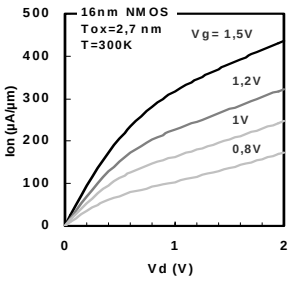


Fig. 7.

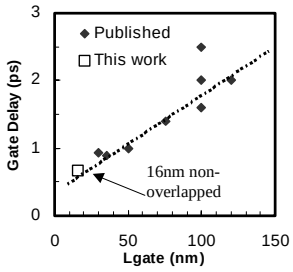


Fig. 8.

5. Silicon On Nothing

SiGe may also be used as a sacrificial layer for fabricating thin-body SON (Silicon On Nothing), [22], single- and double-gate devices. Exclusive and unique advantage of SiGe for this application consists in the combination of its capacity of transferring the lattice continuity between the Si-substrate and the Si-cap layer and the possibility of its selective etching once the transfer is accomplished. Fig. 9 illustrates the most representative SON process step – the gate stack bridging over an empty tunnel (that gives the name to the process, even if for CMOS applications the tunnel will be eventually filled with dielectric). Thanks to the thinness of the conducting film, 20nm in the example shown in Fig. 10, extremely high electrical performance has been demonstrated on SON transistors Fig. 11. More recently, we have demonstrated [24] highly performant SON channels as thin as 5nm.

The SON process has also been successfully applied to fabrication of DG planar devices [25].

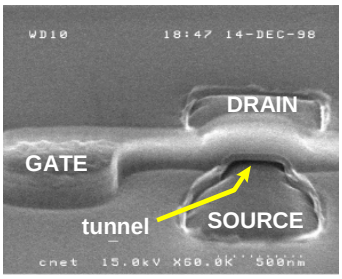


Fig. 9.

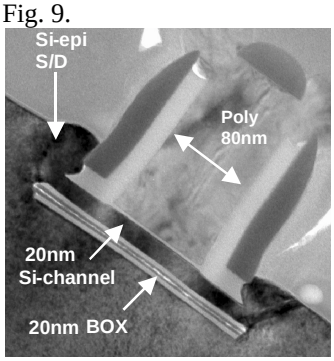


Fig. 10.

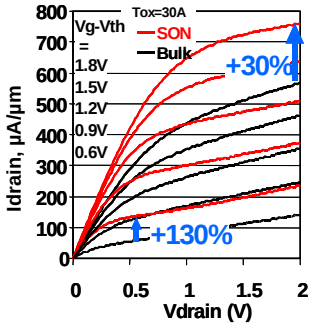


Fig. 11.

Fig. 9. SON name-giving step – gate stack over an empty tunnel, [22].
Fig. 10. Perfect SON MOSFETmorphology, [23].
Fig. 11. Comparison of output characteristics between SON and bulk 80nm NMOSFETs , [23].

6. Conclusions

No other material can compete with SiGe on the spectrum of applications, and probably none can claim, as can SiGe, to be equally useful when present or when absent. In this paper, we have reviewed many intriguing applications, and illustrated their value and potential for advanced CMOS applications by experimental morphological and electrical results.

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