Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 292-293

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Oxidation-Induced Damages on Germanium MIS Capacitors with HfO_2 Gate Dielectrics

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1. Introduction

Since the high-k dielectric films are usually grown by deposition method, a channel material for high-k FETs is not necessarily required to be silicon. On the other hand, germanium is attractive because of its higher intrinsic mobility than silicon. Then high-k/Ge FET [1] is of a great interest for the low power & high performance application. However, due to the thermodynamically and chemically unstable nature of Ge native oxide, the interface control at high-k/Ge should be more challenging than that at high-k/Si. This paper reports effects of the interface layer formation and of the oxidation-induced interface degradation on HfO_2/Ge capacitor characteristics.

2. Fabrication Process

Both p-type and n-type Ge (100) wafers were used. They were cleaned with isopropylalchol, followed by a dipping into 5% HF solution and rinsed in de-ionized water. The HfO_2 films were deposited by the reactive sputtering of Hf metal in O_2/Ar gas. Two types of film deposition process as shown in **Fig. 1** were conducted: *(A)* HfO_2 deposition directly on Ge substrate, *(B)* HfO_2 deposition just after the formation of 1.5nm Hf-metal layer on Ge in the same chamber. This metal layer was expected to be oxidized during the reactive sputtering and post-deposition annealing and to restrict the growth of interface layer [2]. The thicknesses of as-deposited films were determined to be 10.3 nm for process *(A)* and 9.3nm for process *(B)* by the grazing incident X-ray reflectivity measurement. The post-deposition annealing in pure N_2 or 0.1%-O_2+N_2 mixture ambient was performed from 400ºC to 600ºC. Finally, Au was evaporated to form a Au/HfO_2/Ge MIS capacitor. The capacitors on HF-last Si substrates were also fabricated by the same process to make a comparison.

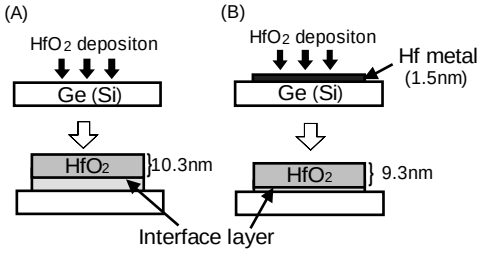

Fig.1 Schematic of the two film fabrication processes. *(A)* Deposition of HfO_2 film directly on Ge (Si) substrate. *(B)* HfO_2 deposition on 1.5nm-thick Hf metal layer on the substrate, which can provide a HfO_2 film with thinner interface layer than process *(A)*.

3. Results and Discussion

In order to find out the proper annealing conditions, the annealing temperature effect was first investigated. **Fig 2** shows a comparison of Ge/Hf ratio by SIMS measurement in HfO_2 films on Ge between before and after annealing in N_2 ambient at 400ºC and 600ºC. No profile change of Ge/Hf ratio was observed by annealing at 400ºC, while Ge diffusion into HfO_2 was clearly observed by annealing at 600ºC. This fact recommends the low-temperature fabrication process to realize HfO_2/Ge devices. Thus we fixed the annealing temperature at 400ºC in this study.

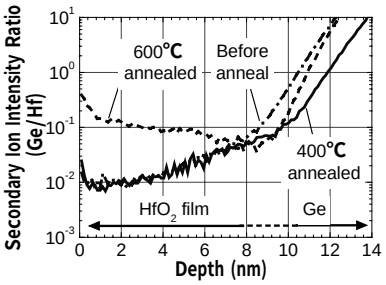

Fig.2 Ge/Hf ratio in HfO_2 films on Ge substrate measured by SIMS. The diffusion of Ge into HfO_2 was significant by 600ºC annealing, while no change of Ge/Hf was detected by 400ºC annealing.

Next, we investigated C-V characteristics of the capacitors fabricated by process *(A)* with N_2 annealing. As shown in **Fig.3** The Ge capacitor shows a significant dependence on the measurement frequency, differing from Si capacitor fabricated by the same process. This fact can be partly explained by the fast minority carrier generation in Ge due to a smaller band gap of Ge. The observed V_{FB} shift (ΔV_{FB}) was as large as –0.89V on Ge, while ΔV_{FB} on Si was below 0.1V. We consider this large ΔV_{FB} comes from the fixed positive charges in the interface layer on Ge. The interface layer was confirmed to be germanium oxide (or hafnium-germanium mixed oxide) from the FT-IR spectra of 20nm-thick films prepared by the same conditions on both substrates (without annealing), as shown

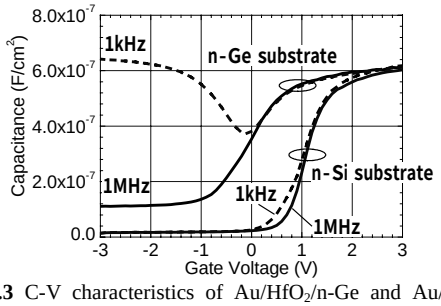

Fig.3 C-V characteristics of Au/HfO_2/n-Ge and Au/HfO_2/n-Si MOS capacitors prepared by process *(A)* with N_2 annealing at 400ºC. For Ge capacitor, quite a large V_{FB} shift (-0.89V) was observed. The prompt generation of minority carriers in Ge can explain a frequency dependent C-V characteristics.

in **Fig.4**. The peaks around 1050cm^{-1} for the film on Si and 850 cm^{-1} on Ge correspond to the asymmetric stretching modes of Si-O and Ge-O [3] respectively, although the peak positions were slightly shifted toward lower wavenumbers compared to those of bulk oxides possibly due to ultra-thin layers.

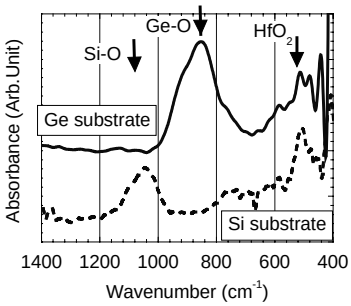

Fig.4 The FT-IR spectra of 20nm-thick film prepared by the same conditions as process *(A)* on both Ge and Si substrates (before annealing). The peaks corresponding to the asymmetric stretching modes of Ge-O and Si-O bonds indicate the formation of their interface layers. The peak observed around 500 cm^{-1} is attributable to HfO_2 [4].

In order to minimize the growth of germanium oxide layer at the interface, the fabrication process *(B)* was examined. **Fig.5(a)** shows CET as small as 2.8nm, and the electrical equivalent oxide thickness (t_{eq}) of the interface layer was successfully decreased from 2.6nm of *(A)* to 0.2nm of *(B)*, which indicates the Hf-metal base layer significantly prevented the interfacial layer growth at the initial stage of sputtering. At the same time, ΔV_{FB} was improved to –0.5V as shown in **Fig.5(b)**, which supports our consideration that interface layer causes ΔV_{FB}.

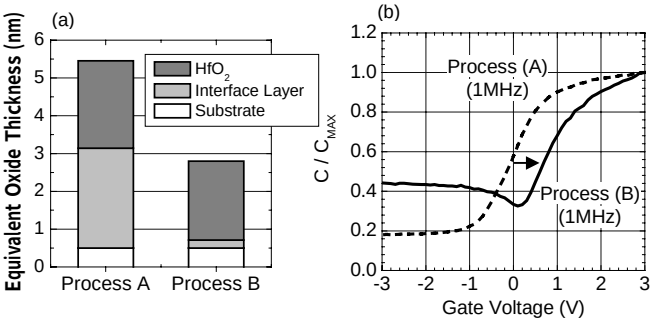

Fig.5 Difference of (a) electrical equivalent thickness (t_{eq}), and (b) C-V characteristics in the process *(A)* and *(B)*. t_{eq} of the interface layer was estimated to be 2.6nm for *(A)*, and 0.21nm for *(B)*, by assuming ε_{HfO2} is 18 and t_{eq} for the accumulation layer in the substrate is 0.5nm. Figure (b) shows the normalized C-V characteristics at 1MHz of Au/HfO_2/n-Ge with N_2 annealing at 400ºC. Estimated ΔV_{FB} is –0.89V for *(A)* and -0.5V for (B).

The C-V characteristics for capacitors fabricated on p-Ge by process *(B)* with N_2 annealing at 400ºC are shown in **Fig.6(a)**, which shows almost the same CET, ΔV_{FB}, and frequency dependence as those of n-Ge capacitors. The annealing ambient effects on C-V characteristics are shown in **Fig.6(b)**, where a significant stretch-out of C-V curve is observed for the sample annealed in 0.1%-O_2 ambient compared to that annealed in pure N_2. It suggests that even a slight oxidation can induce the interface degradation, despite of only a little increase of CET. After the forming gas annealing at 400ºC of the 0.1%-O_2 annealed sample, the stretch-out is recovered to the initial state. This would be explainable by the annihilation of the oxidation-induced defects. A possible model for the degradation and annihilation of the defects is schematically shown in **Fig.**7. The oxidation process may promptly induce impure oxides with a number of dangling bonds at Ge surface, which can be passivated by the forming gas annealing.

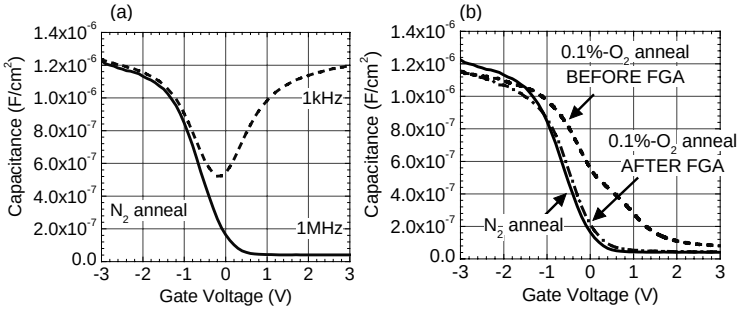

Fig.6 (a):Frequency dependent C-V characteristics of Au/HfO_2/p-Ge fabricated by process *(B)* with N_2 annealing at 400ºC. CET is 2.8nm and ΔV_{FB} is -0.40V. (b):Comparison of 1MHz C-V curve of the sample annealed in different ambient. Annealing in 0.1%-O_2+N_2 (broken line) causes a larger stretching out than annealing in pure N_2 (solid line). This degradation was annihilated by a forming gas annealing at 400ºC (broken and dotted line).

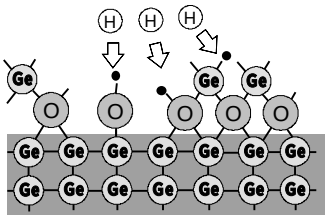

Fig.7 Schematic picture for the oxidation-induced degradation by a formation of dangling bonds at the HfO_2/Ge interface. The forming gas annealing seems to passivate them.

3. Conclusions

Au/HfO_2/p- and n-Ge MIS capacitors were fabricated, and effects of the interface oxidation on the electric characteristics were investigated. The interface germanium oxide layer may be responsible for ΔV_{FB}. In addition, it is inferred that the post-deposition oxidation induces a severe interface degradation. Indeed these results indicate that the precise oxygen control at HfO_2/Ge interface is very challenging for HfO_2/Ge systems, but very nice C-V characteristics observed both for n- and p-Ge capacitors show a promising possibility of achieving high-performance & low voltage high-k/Ge CMOS devices.

Acknowledgements

This work was partly supported by NEDO/MIRAI project.

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