Performance Estimation and Benchmarking for Carbon Nanotube FETs and Nanodiode Arrays

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1. Introduction

Molecular devices including carbon nanotube FETs [1], and those based on semiconductor nanowires [2] and single or few number of molecules [3] have received much attention over the last few years. While some of these new devices have achieved experimental results that may rival some of the best silicon FETs [4], most of these devices have yet to show electrical characteristics beyond the basic, functional level. In this paper, we present an analysis of the potential performance of carbon nanotube FET and nanodiode arrays. We also benchmark the performance of these devices against Si CMOS.

2. Field-Effect Transistors (FETs)

Molecular FETs based on carbon nanotubes [1] and semiconductor nanowires [2] have been demonstrated. The early reports focused on individual transistor on/off currents and their ratio. However, the on/off ratio by itself is not a sufficient performance measure. One characteristic of molecular devices is that the width of the conducting channel is not a continuous variable and is sometimes ill-defined (e.g. in a single-molecule channel). In order to compare with Si FETs, it was proposed to normalize the current to an effective width occupied by an array of tubes/wires/molecules [5]. Fig. 2 shows one of the highest current drive CNFETs [6] plotted in comparison with optimized Si FETs [7]. The current is normalized to a per-unit device width basis assuming an effective device width of $\pi r^2$ ("r" is the radius of the nanotube). The CNFET exhibits minimal current degradation at high gate bias and corresponding high carrier density. This is unlike Si FETs where high gate bias is accompanied by significantly degraded mobility due to surface roughness scattering. The subthreshold slope is about 80 mV/decade, indicating that an efficient gate field coupling is possible (unlike earlier devices with thicker gate insulators). The output conductance, despite the use of a fairly long channel (1400 nm), is higher than expected. The normalized current drive and the saturation transconductance ($G_{\text{sat}}$) are high as compared to Si FET. A more suitable performance assessment should also account for the differences of the gate capacitance (Fig. 1) [4]. Both $G_{\text{sat}}/C$ and CV/I take into account the input gate capacitance and are independent of the effective device width normalization. If one assumes that one can reduce the gate length while maintaining its current drive, then the CV/I of CNFETs are quite comparable to well-optimized Si FETs even at this early stage of development [4] (Fig. 3). For Si FET, the gate capacitance (C) in both the $G_{\text{sat}}/C$ and CV/I metrics has a direct correlation with the saturation current (I) and the saturation transconductance ($G_{\text{sat}}$). For carbon nanotubes, semiconductor nanowires, and other molecular FETs, this correlation may not exist due to the possibility of ballistic transport and the dominance of the contact (e.g. Schottky barrier (SB) [8]) on current injection into the channel. The usual scaling of the saturation transconductance and the saturation current with the gate capacitance in Si FET may not be applicable for molecular devices in general. However, the CV/I metric still has relevance since the gate capacitance represents the effectiveness of gate voltage coupling to the channel. It is also the load capacitance for the preceding logic stage. The subthreshold slope, a measure of device performance (power consumption), is dominated by the SB due to the relatively thick gate insulator used in today’s CNFET. The device scaling potential of CNFETs has yet to be further elucidated. The electrostatics of CNFET is different from Si FET due to the SB contact and 1D channel [8]. Experimental progress has been stymied by inadequate reproducibility of the contact.

Since a single nanotube carries little current drive, in order for CNFETs to deliver current for driving long capacitive interconnect wires, an array of carbon nanotubes is required. For an array, electrostatic screening (Fig. 4) can reduce gate capacitance by more than a factor of two when the gate dielectrics associated with individual nanotubes are merged in a tight pitch ($p < 2(\pi r)$) array [9]. Similar considerations apply to nanowire and molecular FETs.

Historically, device footprint of Si FETs has followed lithography scaling. The length of a minimum-sized transistor (Fig. 5) is about 5 – 6× larger than the gate length for a contacted-pitch transistor (without isolation, with shared source/drain as in a stacked NAND), and about 10 – 12× the gate length for an isolated transistor, resulting in a device area of 8F² and 16F², respectively [10]. When wiring and devices with W/L>1 are included, average device footprints are about 25 – 64 F², depending on circuit style and loading. For FETs based on nanotubes, nanowires, and molecules, the device footprint will follow historical trends since the same device considerations (tunneling, electrostatics, device structure) apply.

3. Diode Arrays

Diodes arranged in a crossbar array have been proposed as ultra-high density molecular devices requiring only simple fabrication processes [11]. General logic functions can be performed with such ROM-base architectures as a
programmable logic array (PLA) [12]. It is conceivable that the diode array can be made with a half-pitch (F) smaller than the general lithographic half-pitch (F) using self-assembly or other chemical synthesis methods. The ratio of device density of contacted-pitch transistors to diodes of a PLA array is ~8F/4F2, which can be substantial (128 for F/H2=8). To compare diode PLAs with random transistor logic, we must include the buffer transistors of the PLA and consider the same logic function (more diodes are needed to perform the same logic function as transistors). For an example of a 2-bit adder, the PLA requires a 11 × 11 array plus buffer transistors, while static (dynamic) CMOS gates require 54 (33) transistors [13]. Fig. 6 shows a representative comparison, with details depending on transistor sizing (for driving loads) and complexity of the function implemented. The density advantage of the diode PLA is largest when F/H2 is large. Since the area of the buffer transistors of the diode PLA is substantial, reducing H2 is effective for area reduction only up to a point. Tunneling between neighboring wires also places a limit on the F/H2 ratio.

3. Conclusions

We present a preliminary estimate of the performance of carbon nanotube and other molecular devices, and benchmark the performance against Si FET. While CNFET (and other FET-based molecular devices) offers potentials for better speed/power trade-off, device density may remain comparable with Si FETs. Crossbar diode arrays may offer density advantage if the diode arrays can be made with a finer pitch, perhaps by using self-assembly methods. However, the density advantage is much smaller at the functional block level than the raw device footprints indicate. The speed-power trade-off of diode PLA arrays needs to be further examined.

References


![Fig. 1 Comparison of selected device characteristics of CNFETs and Si FETs. CNFET saturation current and transconductance are normalized to an effective device width of "4r".](image1)

![Fig. 2 I-V characteristics of the electrolyte-gated p-CNFET [6] at room temperature compared to Si FET [7].](image2)

![Fig. 3 CV/I delay of Si FET and CNFET. Projection for CNFET assumes gate length is reduced to 50 nm with no change in current drive from long-channel data.](image3)

![Fig. 4 Gate capacitance vs. pitch for a top-gated CNFET. The gate dielectric has thickness t, and the nanotube radius is r. Solid symbols: r=0.7 nm. Open symbols: r=1.5 nm. Inset: potential contours for r=0.7 nm, pitch=1.68 nm. Potential lines are in 100 mV increments.](image4)

![Fig. 5 Length of a minimum-sized transistor in multiples of gate lengths.](image5)

![Fig. 6 Area of a 2-bit adder implemented using diode PLA (and minimum sized buffer transistors) and conventional CMOS logic gates. A larger diode array pushes the curve toward the right. Larger transistor sizes push the curve up.](image6)