

Thermal Instability of Poly-Si Gate Al₂O₃ MOSFETs

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1. Introduction

For low standby power and high performance logic applications, high-k gate dielectrics are required as an alternative to SiO₂ or SiON because of their low gate leakage current and higher dielectric constant. But despite of much work, critical issues such as the thermal stability, mobility degradation and reliability still remain unsolved.

It has been reported that an interfacial SiO₂ layer is effective in suppressing the mobility degradation of Al₂O₃ MOSFETs [1]. However, the effects of the stability of SiO₂/Al₂O₃ on the MOSFET characteristics have not been studied. In this paper, we address the thermal stability of poly-Si gate SiO₂/Al₂O₃ MOSFETs under high temperature post deposition annealing (PDA) and activation annealing (RTA).

2. Device Fabrication

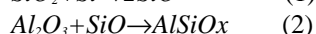
We have fabricated capacitors and transistors using a poly-Si/Al₂O₃/SiO₂ gate stack. An interfacial 0.9nm-thick SiO₂ (or SiON) layer and an ALD Al₂O₃ were grown on 300mm wafer with recessed LOCOS. After PDA (O₂ 0.2%), a 150nm a-Si layer was deposited. After gate definition, RTA was applied. Finally H₂ sintering was performed. For transistors, conventional CMOS processes were applied.

3. Results and Discussion

PDA temperature dependence: interface instability

The PDA temperature dependence of the C-V characteristics is shown in Fig. 1. As the PDA temperature decreases, the capacitance increases (Fig. 1). As shown in Fig. 2, the electrical thickness of the interfacial SiO₂ layer decreases in the case of low temperature PDA or when no PDA was carried out. In spite of the fact that the initial SiO₂ thickness was about 0.9nm, the interfacial layer thickness after processing became about 0.3nm for the case in which no PDA was done. The variation in the interfacial layer thickness with PDA temperature was confirmed by TEM (Fig. 3), and good agreement between the electrical and physical thicknesses was obtained (Fig. 4).

The ATR spectra suggest that an Al-silicate layer is formed after RTA and the amount of silicate increases with decreasing PDA temperature (Fig. 5). The process for the formation of silicate is considered to be as follows [2],



Although a lower EOT is obtained with a low temperature

PDA, the pMOSFET subthreshold characteristic is degraded (Fig. 6). It is believed to be due to the penetration of B from the poly-Si gate to the channel because there is little change of swing in the nMOSFET. Charge pumping measurements indicate the occurrence of defect generation and/or interfacial roughening during reduction of the SiO₂ [3] and Al-silicate formation in case of low temperature PDA, which results in degradation of the mobility (Fig. 7). Al diffusion into the channel was reported to be another cause of mobility degradation [4]; however, it was shown to be not significant in our samples (Fig. 8).

RTA temperature dependence

Although good mobility (>300cm²/V.s) was obtained with high temperature PDA, the mobility was degraded if the RTA temperature was higher than 1000°C (Fig. 9). This is believed to be mainly due to diffusion of dopant into the gate dielectric. The time zero dielectric breakdown (TZDB) characteristics accord with the mobility data (Fig. 10).

Interfacial oxide layer dependence

The high temperature thermal treatment significantly affects the uniformity of the MOSFET characteristics. With a SiO₂ interfacial layer, there is a large variation in the C-V curves after high temperature PDA/RTA (Fig. 11). A SiON interfacial layer is effective in improving the uniformity of the C-V curves even after a 1050°C PDA/RTA. Similarly, the TZDB characteristics with a SiON interfacial layer are better than those with a SiO₂ interfacial layer (Fig. 12). This indicates that the reliability of the Al₂O₃/SiO₂ (or SiON) depends on the quality of the interfacial oxide.

4. Conclusions

A SiO₂/Al₂O₃ dielectric stack is found to be unstable under high temperature RTA (1050°C) after poly-Si gate deposition. The PDA temperature should be higher than RTA temperature in order to suppress the reaction at the interface, which severely degrades the MOSFET characteristics. As a result of interfacial oxide degradation by diffusion of dopant, the mobility and reliability of the MOSFET are degraded. We have demonstrated that high mobility and good uniformity can be obtained with a 1050°C PDA and a 950°C RTA on 130nm CMOSFETs.

References

- [1] S. Saito, et al., SSDM, 704(2002)
- [2] T.S. Jeon, et al., Appl. Phys. Lett. 78, 368(2001)
- [3] M. Copel, et al., Appl. Phys. Lett. 78, 2670(2001)
- [4] S. Guha, et al., Appl. Phys. Lett. 81, 2956(2002)

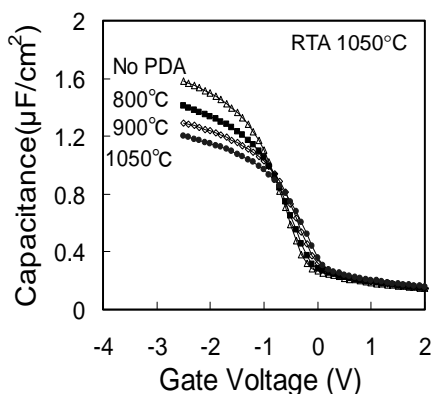


Fig. 1 PDA temperature dependence of C-V curves. SiO₂ 0.9nm/Al₂O₃ 3nm.

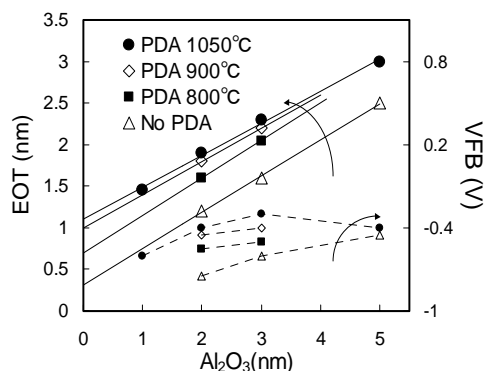


Fig. 2 Summary of EOT and V_{FB} versus Al₂O₃ thickness.

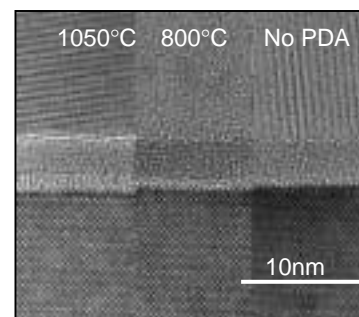


Fig. 3 TEM images: PDA temperature dependence (RTA 1050°C).

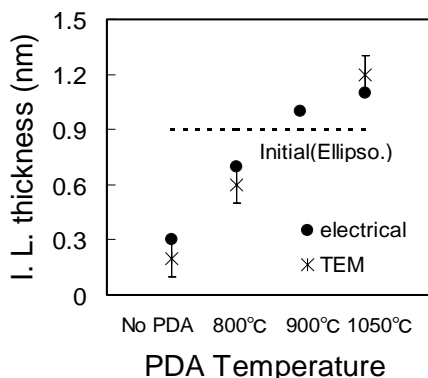


Fig. 4 The interfacial layer thickness dependence on PDA temperature.

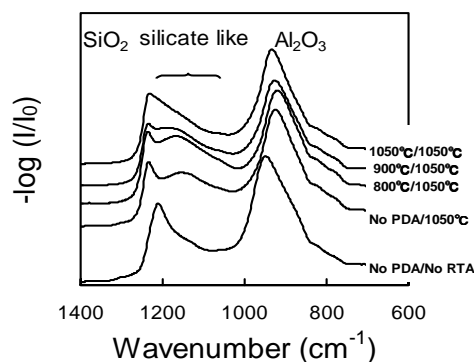


Fig. 5 ATR spectra of SiO₂ 0.9nm/Al₂O₃ 3nm /a-Si.

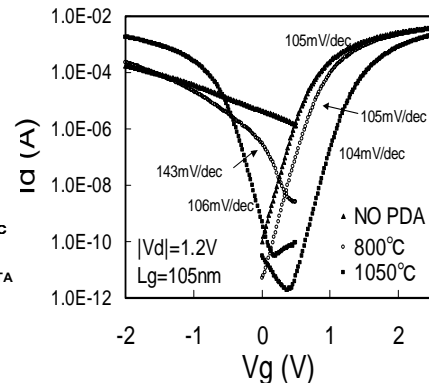


Fig. 6 Subthreshold characteristics of n and pMOSFETs.

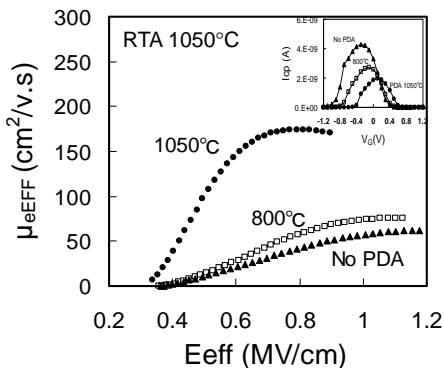


Fig. 7 Mobility and charge pumping (in set) dependence on PDA process.

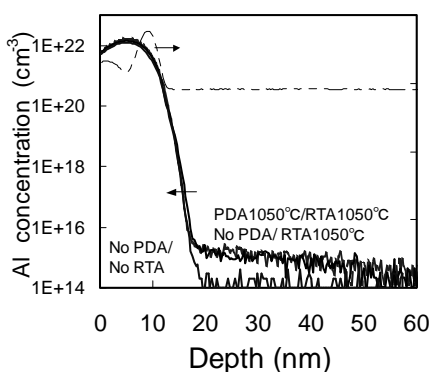


Fig. 9 Al depth profile measured by BSIMS.

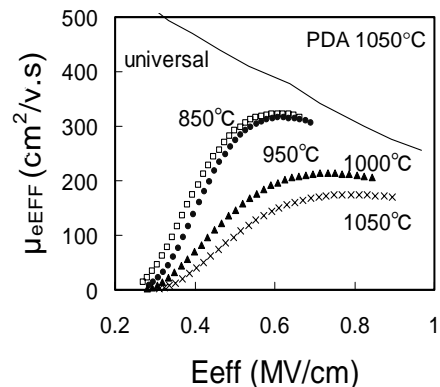


Fig. 10 RTA temperature dependence of electron mobility.

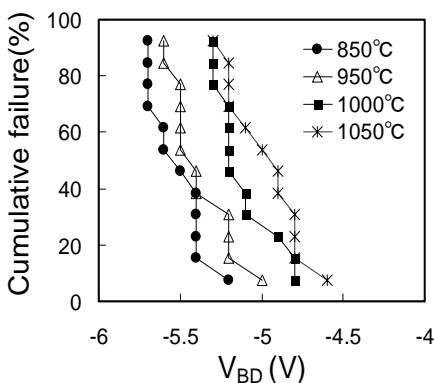


Fig. 10 RTA temperature dependence of TZDB (PDA 1050°C).

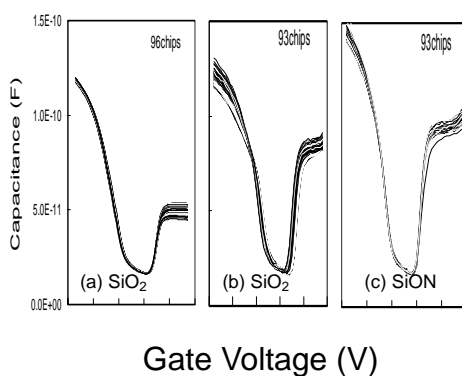


Fig. 11 C-V curves: (a) PDA 800°C/RTA 850°C, (b)(c) 1050°C PDA/RTA

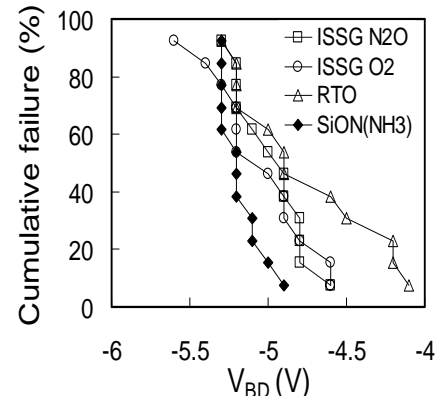


Fig. 12 Interfacial layer dependence of TZDB.