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Advanced SiGe-free Strained Si on Insulator Substrates: Thermal Stability and Carrier Mobility Enhancement

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1. Introduction

SiGe-free strained Si on insulator (SSOI) is a groundbreaking platform for Si-based CMOS that combines the advantages of strained Si and Si on insulator (SOI) technologies. The initial reports of the fabrication process, thermal stability, and physical characterization of SSOI have been described previously with the wafer fabrication process illustrated in figure 1. [1,2] This article describes the latest advances in material quality and process stability of 20% and 30% Ge strain equivalent SSOI substrates, as well as the first observations of carrier mobility enhancement in SiGe-free SSOI.

2. Results and discussion

Figure 2 shows a picture of a finished 150 mm 400Å SSOI wafer with excellent visual uniformity. Figure 3 is a spectroscopic ellipsometry (SE) map of a 20% 400Å SSOI wafer with a strained Si thickness uniformity of +/-7.9% (σ = 5.8%) while figure 4 is an SE map of a 30% 500Å SSOI wafer with a strained Si thickness uniformity of +/-7.0% (σ = 3.3%). All wafers were prepared with 1000Å buried oxide (BOX) layers, and 20% and 30% refer to the approximate Ge content of the bulk strained Si wafers from which the SSOI layers were transferred. These results demonstrate the SiGe removal process yields good uniformity of the final SSOI layer. Uniformity will be further improved by refinements in the initial epitaxy and SiGe removal process. Figure 5 shows a 1×1 μm AFM surface scan of a finished 20% SSOI wafer surface. The 1×1 μm RMS is 0.49 nm while the 10×10 μm RMS is 0.72 nm.

In addition, the thermal stability of SSOI was evaluated after several different thermal treatments in an N_2 ambient at temperatures of 950-1100ºC and times of 3-400 minutes. For each anneal cycle, samples were loaded at 600ºC, and the temperature was ramped to the final temperature at a rate of 5ºC/min. The perpendicular and parallel lattice constants and strains were measured by asymmetric {224} triple axis x-ray diffraction reciprocal space maps after annealing. [3] Figure 6 shows a reciprocal space map of a 30% SSOI sample annealed for 45 minutes at 1050ºC with clearly visible strained Si and Si substrate peaks. Figure 7 shows the strain levels of 20% and 30% SSOI materials after annealing. Note that no significant strain relaxation occurs in these samples for any thermal treatment studied, indicating that the strain is very thermally stable. These strain levels are consistent with the expected 1.26% parallel strain induced by the $Si_{0.68}Ge_{0.32}$ template for 30% SSOI and the 0.796% strain induced by the $Si_{0.79}Ge_{0.21}$ template for 20% SSOI. In addition, Raman spectroscopy was used to confirm the strain stability on the 20% SSOI samples annealed at 1000ºC and 1050ºC. Thus, both techniques confirm that the SSOI structure maintains its tensile strain level in the absence of the relaxed SiGe layer during thermal treatments much more aggressive than those commonly utilized in state-of-the-art CMOS processes. In comparison, strained Si on strain-inducing SiGe films would be severely compromised by Ge diffusion during these aggressive thermal budgets. This extraordinary thermal stability, vastly improved over that observed in initial SSOI reports, is a direct result of recent improvements in the SSOI fabrication process.

A mercury-based pseudoMOSFET [4] was used to determine the electrical properties of 20% SSOI material. The transistor output characteristic in figure 8 shows good transistor behavior. The electron mobility extracted by the technique on the SSOI films is 902 cm^2/V-sec, which is considerably higher than the 600-650 cm^2/V-sec measured for standard SOI materials by the same technique. [4] These results demonstrate the carrier mobility enhancement inherent to the SSOI platform.

3. Conclusions

Second generation SSOI substrates with tensile strain levels of 0.8-1.26%, Si thickness uniformities of better than 8%, vastly improved thermal stability, and electron mobility enhancements of 40-50% over standard SOI have been demonstrated. The improvements in SSOI material quality are a direct result of the use of high quality bulk strained Si starting substrates and improvements in the SSOI fabrication process. The tensile strain level and concomitant carrier mobility enhancement of these SSOI substrates are maintained even after annealing at 1100ºC for ~80 minutes, reaffirming the suitability of SSOI as a next-generation platform for Si CMOS.

Acknowledgements

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References

[1] T. A. Langdo, et al., IEEE International SOI Conf. Proc., 211 (2002).
[2] T. A. Langdo, et al., Appl. Phys. Lett. **82**, 4256 (2003).
[3] M. Erdtmann, et al., SSDM 2003.
[4] H. J. Hovel, Solid State Elec. **47**, 1311 (2003).

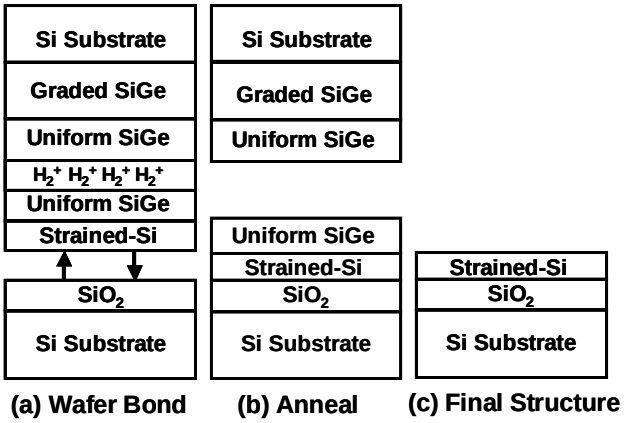

Figure 1: SSOI fabrication process: a) wafer bond b) anneal c) SiGe removal and final structure

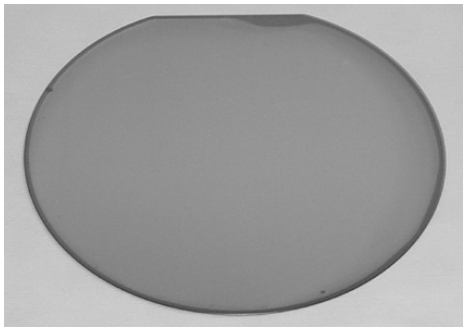

Figure 2: 150 mm 400Å 20% SSOI wafer

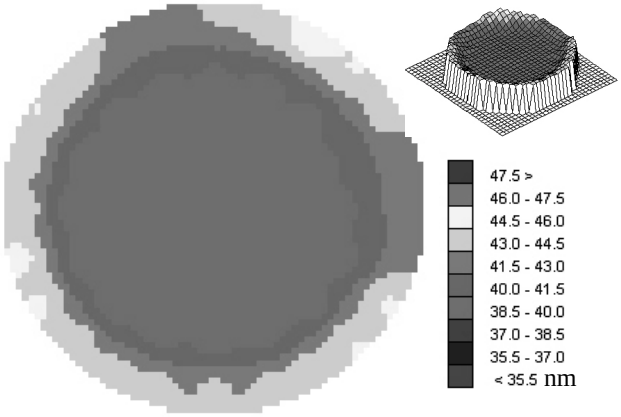

Figure 3: 20% SSOI spectroscopic ellipsometry map

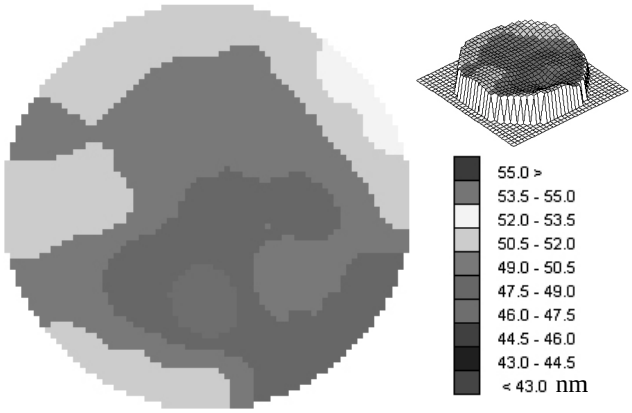

Figure 4: 30% SSOI spectroscopic ellipsometry map

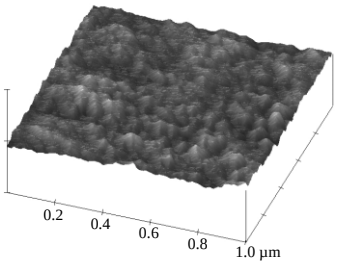

Figure 5: 20% 400 Å SSOI 1×1 µm AFM scan

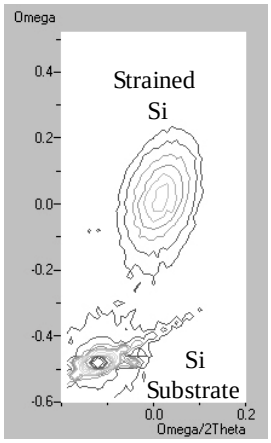

Figure 6: 30% 500 Å SSOI x-ray reciprocal space map

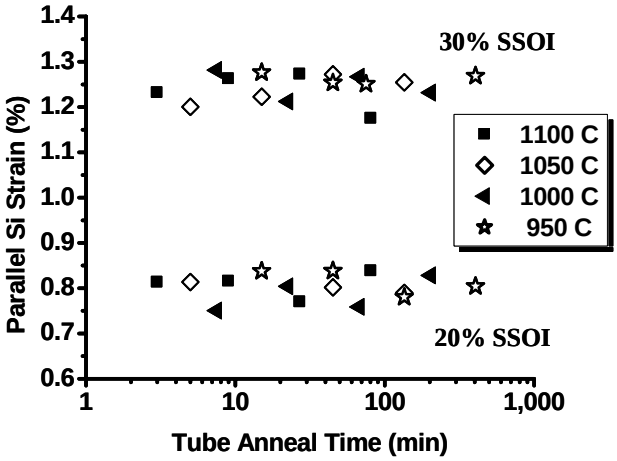

Figure 7: 20% SSOI and 30% SSOI strain thermal stability

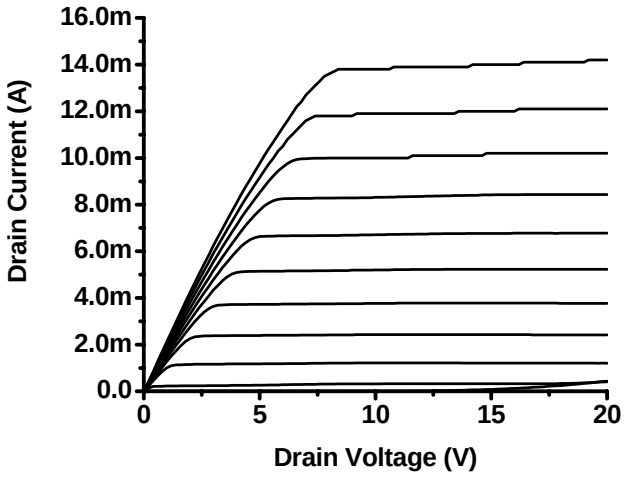

Figure 8: 20% SSOI HgFET output characteristic