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Electronic and photonic devices via one-dimensional stacking of quantum structures

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1. Introduction

Materials and devices incorporating quantum structures and reduced dimensionality are attracting increased attention. In this talk I will discuss the interest in and the challenge of realizing one-dimensionally arranged heterostructures, such as quantum dots and tunnel barriers. I will concentrate my presentation on the formation, properties and applications of semiconductor nanowires in general, and heterostructures in nanowires in particular, and will, when appropriate, make comparisons with self-assembled quantum dots functioning as active elements in tunneling devices or seen as ideal quantum emitters.

2. Results for growth and properties of nanowires.

I will start up with a description of the vapor-liquid-solid (VLS) growth mode for formation of III-V semiconductor nanowires from catalytic nanoparticles. I will then show examples of how this method has allowed us to grow nanowires of GaAs with control of diameter, position and orientation of the nanowires using aerosol gold nanoparticles as monodisperse catalytic nuclei controlling growth. It is found that the most common orientation of VLS-grown nanowires is in the <111>B-direction, in which case the shape of the nanowires is a rod with a hexagonal cross-section. Under some circumstances it is possible to orient the nanowires in <001>. In Figure 1 is shown the way nanowire dimensions as well as nucleation sites for the formation of GaAs nanowires can be controlled. Here an aerosol technique was used providing monodisperse gold nanoparticles and nucleation sites were controlled by AFM-manipulation of such gold nanoparticles.

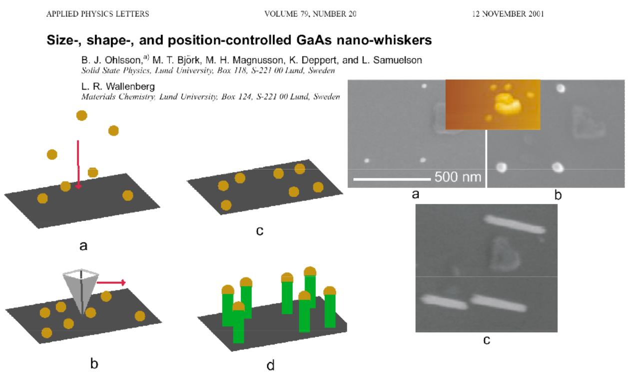


Fig. 1 Formation of size, shape and position-controlled GaAs nanowires from gold nanoparticles

The most significant break-through for growth and the interest in semiconductor nanowires has probably arrived with the development of techniques allowing the controlled formation of sharp heterostructure interfaces inside nanowires, hence allowing the composition to be abruptly changed in the length direction of the nanowires. In this way designed one-dimensional potential landscapes may be realized. One year ago we reported the first defect-free and abrupt heterostructure interface structures, with analysis of structural properties as well as the energy structure (Fig. 2), studied via thermionic emission of electrons in n-type InAs nanowire containing thick (≈100 nm) barriers of InP. We could in this way determine the band-offset in the conduction band between InAs and InP to be about 0.6eV.

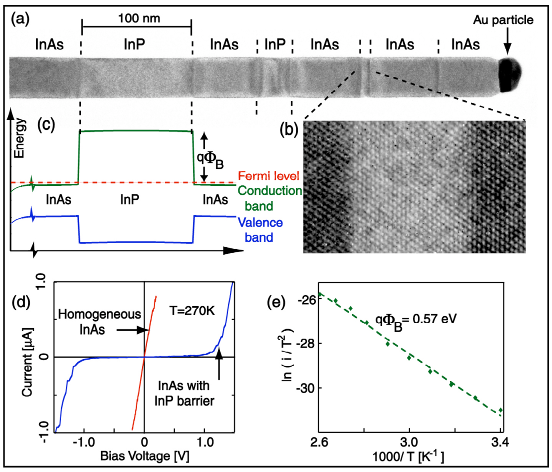
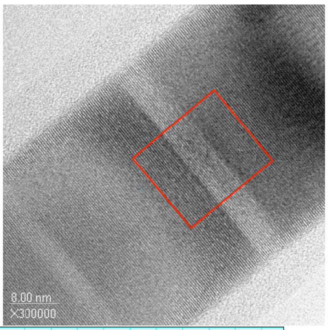


Fig. 2 TEM-images of InAs nanowire containing a series of barriers of InP.. Transport of electrons across thick barriers occur via thermionic emission over the barrier, the hight of which is determined to be about 0.6 eV.

With the possibility of realizing ideal heterostructures in one-dimensional nanowires it becomes possible to create new types of electronic and photonic devices. The first examples of such devices were published recently when we reported 1D-0D-1D resonant tunneling devices formed inside nanowires, in which emitter, QD and collector structures were formed in InAs, with InP as barriers. Examples of the results obtained are shown in Fig. 2 and 3, with example of high-resolution TEM image of a single barrier in Fig. 2 and with the device energy structure and the resulting IV-characteristics shown in Fig. 3.

TEM-analysis of a single InP barrier in an InAs nanowire

A high-resolution TEM image of an InAs whisker grown in the <111> direction with two InP barriers. The average spacing between the lattice fringes in the lighter band is 0.344 nm, corresponding well to d111= 0.338 nm of InP. Below is shown a one-dim integrated profile of the boxed area. The width of the barrier is about 5.5 nm (11 lattice spacings), and the interface sharpness in the order of 1-3 lattice spacings, judged by the jump in image contrast. The background is not linear due to bend and strain contrast around the interfaces.



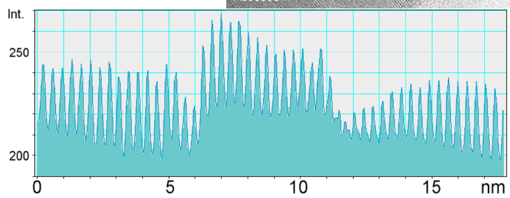


Fig. 3 High-resolution TEM-images of single barrier of InP in a nanowire of InAs, from which barrier thicknesses can be determined with high degree of accuracy.

First implementation of a 1D heterostructure nanoelectronic device in a nanowire as a double-barrier resonant tunneling diode (DBRTD) in InAs with InP barriers.

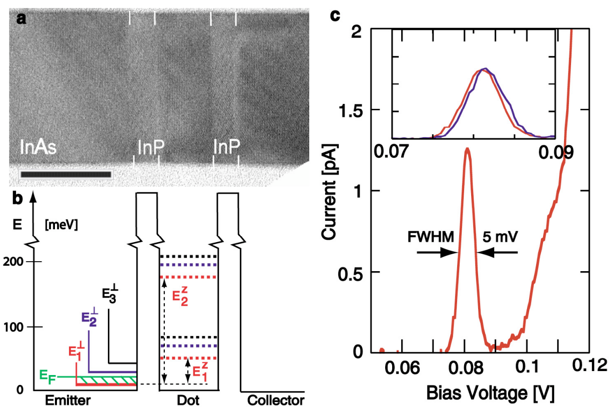


Fig. 4 A double-barrier resonant tunneling device realized via bottom-up growth of an InAs nanowire with InP barriers. The IV-characteristics show ideal tunneling characteristics via the InAs QD as expected for the energy band structure (left).

Besides these already published results I will present novel results from heterostructures formed in nanowires, e.g. for single-electron transistor (SET) structures created in structures similar to the resonant tunneling devices shown above, but with adjusted size of the coulomb island, by which the sequential charging of the island can be controlled and studied. I will also show new results from luminescence from single quantum dots formed in single nanowires, allowing the observation of sharp exciton luminescence of a quality similar to that found in SK QDs. All the results described so far have been obtained by chemical beam epitaxy, i.e. growth under UHV-conditions using metal-organic precursors. Towards the end of my presentation I will also describe very recent results obtained by low-pressure MOVPE growth, resulting in well controlled nucleation and growth of GaAs and InP nanowires, including formation of 2D arrays of nanowires.

3. Conclusions:

Bottom-up fabrication via vapor-liquid-solid growth allows the formation of ideal and defect-free semiconductor nanowires with control of size, shape and position of the wires. In this talk is also presented that this method for nanowire growth allows highly accurate control of the formation of heterostructures, allowing the fabrication of one-dimensional devices such as resonant tunneling and single-electron transistor devices as well as single quantum dot emitter device structures.

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