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ZnO Metal-Insulator-Semiconductor Field-Effect-Transistors

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1. Introduction

ZnO is being used for the varistor, gas sensor, transparent electrode and surface acoustic wave devices. These applications are based on ceramics or polycrystalline form of ZnO. Since the ultra-violet (UV) lasing from ZnO nanocrystalline films was observed [1], ZnO has attracted revolutional attention as a direct transition wide bandgap semiconductor. Bandgap engineering was achieved in (Mg, Zn) O alloy [2], enabling as to study multi quantum well structures [3]. For the UV light emitting device application, formation of *p*-type ZnO is the critical issue and has been extensively studied [4]. The *p*-type doping into ZnO was essentially difficult because ZnO shows naturally *n*-type conductivity due to oxygen vacancy and/or interstitial Zn, which tend to compensate holes introduced by acceptor dopants. Instead of impurity doping we have proposed to utilize the field effect doping using metal-insulator-semiconductor field-effect-transistor (MISFET) structure for achieving carrier inversion. An attempton for making ZnO FETs were already performed using bulk single crystal over 30 years ago [5]. Recently, polycrystalline ZnO thin film transistors (TFTs) were reported for the purpose of alternative the amorphous Si TFTs application [6] or demonstration of an invisible transistor [7]. The device performance of those TFTs is limited by existence of grain boundaries in polycrystalline form of the channels. Here we report our preliminary results on single crystalline ZnO channel so as to improve the device performance towards formation of carrier inversion layer.

2. Experiments

300 nm-thick ZnO films were grown by laser molecular-beam epitaxy technique on a lattice matched $ScAlMgO_4$ (mismatch is only 0.09 %) single crystal substrates. Typical growth conditions of ZnO were 700 ^oC of substrate temperature, 1 x 10^{-6} Torr of oxygen partial pressure, 0.8 J/cm^2 of laser fluency, and 10 Hz of laser pulse repetition. All FET patterning processes were done by conventional photolithography through *ex-situ* transfer. After defining ZnO mesa channel, Al (50 nm-thick) was evaporated as the source and drain ohmic contacts. Amorphous AlO_x (a-AlO_x) gate insulator was deposited by electron beam evaporation. Finally Al/Au gate electrode was deposited on the top of the insulator. Additional channel contacts were made for the Hall and four probe measurements. Thus our device has essentially Hall bar geometry. The channel length (L) and width (W) were 220 μm and 60 μm, respectively. Cross sectional view of FET structure was shown in Fig. 1.

3. Results and Discussion

The obtained FETs were characterized using semiconductor parameter analyzer (Agilent 4155C) at room temperature. Figure 2(a) shows the drain current (I_d) versus drain-source voltage (V_{ds}) characteristics with various gate voltages (V_g). In high V_g regime, the pinch-off behavior was not clear. We presume this is due to positive ion residing in the gate insulator from the fact that the accumulation behavior at high V_g depends on V_g sweep rate (not shown). Therefore, the I_d versus V_g characteristics measurements were carried out with low seep late so not as to induce the effect of the mobile ions. The field effect mobility (μ_{FE}) was deduced from saturation regime (gradient of $I_d^{1/2}$ vs. V_g plots) and linear regime (gradient of I_d/V_{ds} vs. V_g plots) described by eq. (1) and (2), respectively.

$$\mu_{FE} = \left(\frac{dI_d^{1/2}}{dV_g} \right)^2 \cdot \frac{2L}{C_g \cdot W} \qquad (1),$$

$$\mu_{FE} = \frac{\mathrm{d}\, I_d / V_{ds}}{\mathrm{d}\, V_g} \cdot \frac{L}{C_g \cdot W} \qquad (2),$$

where C_g was the capacitance of the gate insulator (a-AlO_x). The C_g was deduced from $C_g = \varepsilon_o \cdot \varepsilon_r \cdot d_g^{-1}$ relationship, where ε_o, ε_r and d_g were permittivity in vacuum, dielectric constant of a-AlO_x, and film thickness of a-AlO_x, respectively. The value of ε_r was taken from bulk one (= 9.8). In either case, μ_{FE} is deduced to be about 40 $cm^2 \cdot V^{-1} \cdot s^{-1}$ which is the highest value among the reported value, to our best knowledge. Figure 3 shows the μ_{FE} deduced from differential of $I_d^{1/2}$ vs. V_g plots and I_d/V_{ds} vs. V_g plots. Slightly smaller values of μ_{FE} at high V_g (V_g > 2 V) are attributed to the mobile ions. This effect is also seen as the counter clockwise *I-V* histeresis observed in Fig. 2(b). We have used *in-situ* sputtering as an alternative electron beam evaporation to improve the gate insulator properties. Preliminary results on the test device shows better pinch-off behavior and smaller hysteresis suggesting that *in-situ* process is crucially important to avoid

unintentionally introduced contamination at the interface between the channel and the gate insulator.

4. Conclusions

We have succeeded in fabricating a single crystalline ZnO MISFET having reasonably good performance. The field effect mobility was as high as 40 $cm^2 \cdot V^{-1} \cdot s^{-1}$. In order to obtain *p*-type inversion layer, further improvement of the device fabrication process is necessary.

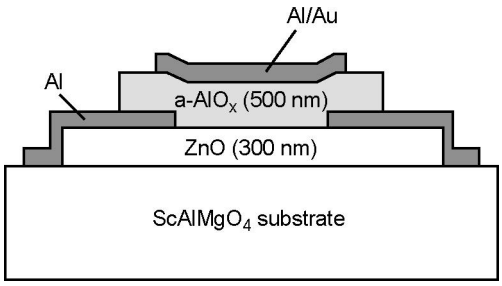

Fig. 1 Cross sectional schematic structure of ZnO MISFET.

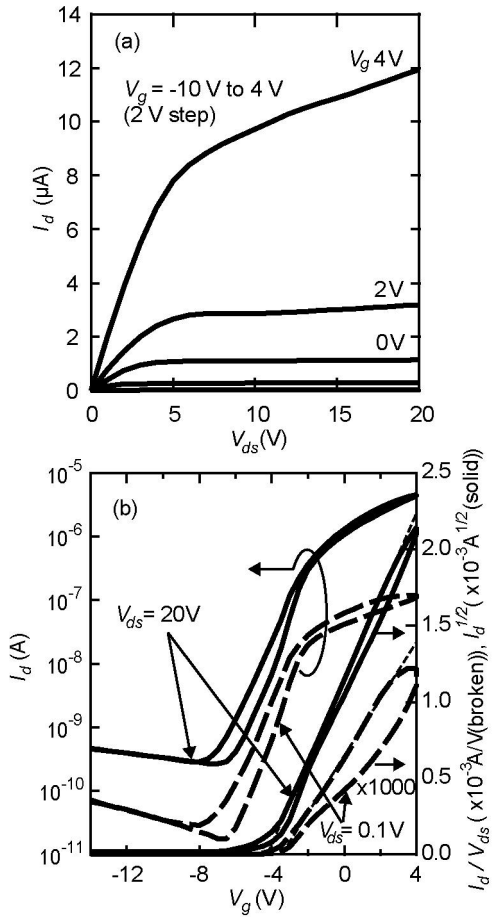

Fig. 2 Typical characteristics of ZnO MISFETs. (a) I_d vs. V_{ds} characteristics at various V_g changed from –10 V to +4 V (+2 V step). (b) I_d vs. V_g characteristics in the saturation regime V_{ds} = 20 V (solid line) and in the linear regime V_{ds} = 0.1 V (broken line). The gradients of $I_d^{1/2}$ vs. V_g plots and I_d/V_{ds} vs. V_g plots were used to deduce the field effect mobility in the saturation regime and the linear regime, respectively.

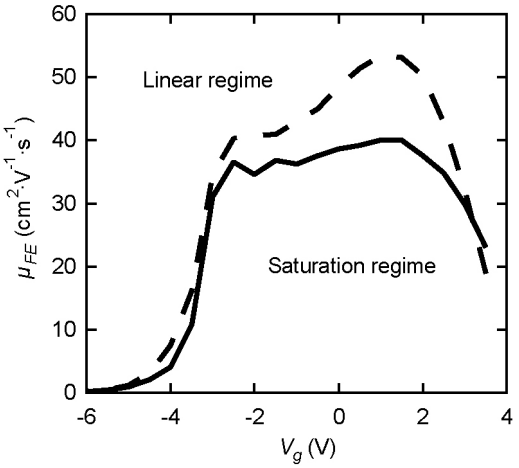

Fig. 3 V_g dependence of the field effect mobility. Solid and broken lines correspond to μ_{FE} in the saturation and linear regimes, respectively. These plots were deduced from the differential of $I_d^{1/2}$ vs. V_g and I_d/V_{ds} vs. V_g relationship measured during sweep down regime (V_g was swept from +4 V to –14 V by –0.5 V step).

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