Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 926-927

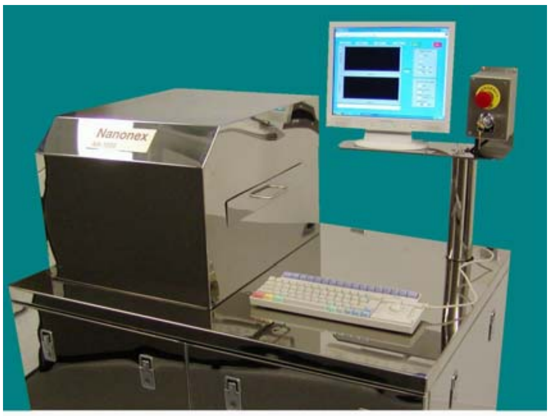
E-6-1 (Invited)

Multi-Level Nanoimprint Lithography For Sub-10 nm, High-Throughput, Low-Cost Patterning

Stephen Y. Chou
Department of Electrical Engineering
Princeton University, Princeton, NJ 08544

Nanoimprint lithography (NIL) pattern nanostructures by a mechanical deformation of materials using a mold. NIL has shown high-throughput, low-cost, and sub-10 nm patterning. The talk will present the state of the art of NIL and its impact to overall nanotechnology development. The latest developments and tools in multi-level nanoimprint lithography will be discussed, as well as laser-assisted direct imprint (LADI). The topic will cover sub-10 nm pattern resolution, high pattern transfer fidelity, excellent CD control, alignment accuracy, and 3D patterning. Fabrications of 60 nm Si MOSFETs on 4” wafers using NIL at all lithography levels, LADI of Si, metals and dielectrics, as well as Nanonex’s nanoimprint lithography tools, resists, masks and processes will also be presented.

Acknowledgement. Thanks to Princeton NSL members and Nanonex.



30 nm Pitch **45 nm Pitch**