# Room-Temperature Observation of Negative Differential Conductance Due to Large Quantum Level Spacing in Silicon Single-Electron Transistor

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# 1. Introduction

Recently, room-temperature (RT) operating silicon single-electron transistors (SETs) have been reported by many groups. The size of the dot in RT-operating SETs is generally less than 10 nm. In such an ultra-small dot, quantum level spacing is not negligible compared to the Coulomb charging energy. As a result, quantum effects such as negative differential conductance (NDC) or current staircase appear in the SET characteristics. These effects have been already observed in silicon SETs [1-4], but the observation temperature was less than 30 K. In order to positively utilize the quantum effects for circuit application, observation at higher temperatures is strongly required.

In this paper, we report the first RT observation of NDC in a silicon multiple-dot SET. The device is an ultra-narrow wire channel MOSFET, which shows large Coulomb blockade (CB) oscillations at RT. The origin of the NDC is considered to be the resonant tunneling due to large quantum level spacing (>  $10k_BT$ ) in the ultra-small dot.

# 2. Fabrication

The device studied in this paper is an ultra-narrow wire channel MOSFET [5]. Figure 1 shows the schematic view of the device. The ultra-narrow wire channel is formed by EB lithography, anisotropic etching using TMAH and isotropic etching using SC1 (NH<sub>4</sub>OH/H<sub>2</sub>O<sub>2</sub>/H<sub>2</sub>O). The channel length is 100 nm and the channel width is less than 5 nm. After wet etching processes, the wire channel is slightly oxidized. The thickness of the thermal oxide is 8 nm. Another 40-nm-thick gate oxide is deposited on the thermal oxide by LP-CVD. Dots (potential wells) and tunneling barriers are self-formed in the ultra-narrow wire channel, and the device acts as a multiple-dot SET [5].

### 3. Measurement

Figure 2 shows the  $I_d$ - $V_g$  characteristics [5]. All the measurements in this paper were performed at RT. Large CB oscillations are observed, and the maximum peak-to-valley current ratio (PVCR) is as high as 6.8. Irregular current peaks indicate that serially coupled dots are formed.

Figure 3 shows the  $I_d$ - $V_{ds}$  characteristics at various  $V_g$ . NDC is observed for positive  $V_{ds}$ , and the fine structure of the current is observed for negative  $V_{ds}$ . This is the first RT observation of NDC in SETs. The PVCR of the NDC at  $V_g$  = 1.7 V is 1.3. Figures 4 and 5 show the contour plot of  $I_d$  and the differential conductance  $(\partial I_d/\partial V_{ds})$ , respectively. CB regions are observed for low  $V_{ds}$ , and NDC regions are observed for high  $V_{ds}$ .

Figure 6 shows the  $I_d$ - $V_g$  characteristics at various  $V_{ds}$ . While many peaks are observed at  $V_{ds} = 0.1$  V, only one peak (at  $V_g \sim 1.3$  V) is observed at  $V_{ds} = 0.8$  V. This fact suggests that this SET consists of an ultra-small dot (dot I) and another dot (dot II) which is larger than dot I. While

CB in both dots contribute to transport for low  $V_{ds}$ , CB only in the smaller dot (dot I) is dominant and almost single-dot SET characteristics are obtained for high  $V_{ds}$ . The peak at  $V_{ds} = 0.1$  V and  $V_g = 1.6$  V shifts to the peak at  $V_{ds} = 0.8$  V and  $V_g = 1.3$  V. This peak shift is indicated by the line A in Fig. 4 and this peak is considered to arise from the dot I.

#### 4. Discussions

Here, we discuss the origin of the NDC observed for positive  $V_{ds}$ . In Fig. 5, the two NDC regions (NDC1 and NDC2) are observed along the line A (peak line of the dot I). The most probable origin of NDC observed in such a region is the resonant tunneling through the dot I [1,6]. Figure 7 shows the schematic diagram of the estimated potential profile in this SET at  $V_g = 1.6 \text{ V}$  (peak of the dot I for low  $V_{ds}$ ). Since the quantum level spacing in the dot I is sufficiently large, electrons in the source can tunnel only to the ground state for N-th electron in the dot I, not to the excited states. When  $V_{ds}$  is low, electrons tunnel to the ground state in the dot I through the relatively thin barrier close to the Fermi level in the source (Fig. 7(a)). As  $V_{ds}$  is increased, the energy levels in the dots fall down. Consequently, electrons must tunnel to the dot I through the thicker barrier close to the conduction band edge in the source (Fig. 7(b)). This decrease in the tunneling rate leads to the decrease in the flowing current and NDC. On the other hand, the NDC regions are separated into the two regions by the line B in Fig. 5. Since the line B stretches from the peak of the dot II (at  $V_g = 1.0 \text{ V}$ ), it is expected that this separation is related to the Coulomb staircase in the dot II. From the voltage range where NDC is observed, the quantum level spacing in the dot I is estimated to be more than 0.25 eV, which is almost ten times the thermal energy at RT.

# 5. Conclusions

We have investigated the electron transport properties of a RT-operating silicon multiple-dot SET. NDC was observed in the SET characteristics at RT for the first time. The observed NDC is attributable to the resonant tunneling due to the large quantum level spacing (>  $10k_BT$ ) in the dot. The result obtained in this study opens up the possibility of circuit application of the quantum effects in SETs.

## References

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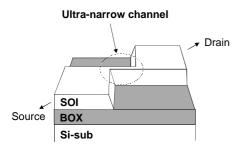


Fig. 1 : Schematic view of the ultra-narrow wire channel MOSFET [5]. A 100-nm-long wire channel is formed by wet etching and slight oxidation.

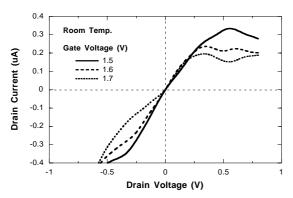


Fig. 3:  $I_d$ - $V_{ds}$  characteristics at various  $V_g$  at RT. NDC is observed for positive  $V_{ds}$  and the fine structure is observed for negative  $V_{ds}$ .

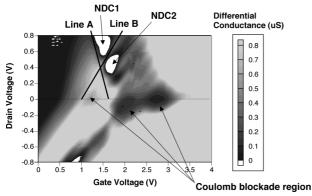
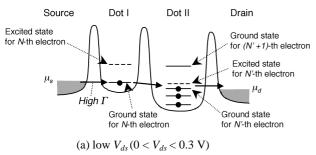


Fig. 5 : Contour plot of the differential conductance  $(\partial I_d/\partial V_{ds})$  at RT. Two NDC regions are observed along the current peak line A.



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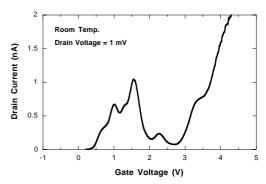


Fig. 2 :  $I_d$ - $V_g$  characteristics at RT [5]. Large CB oscillations with the maximum PVCR of 6.8 are observed.

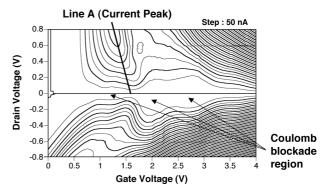


Fig. 4 : Contour plot of  $I_d$  as a function of  $V_g$  and  $V_{ds}$  at RT. CB regions are observed for low  $V_{ds}$ .

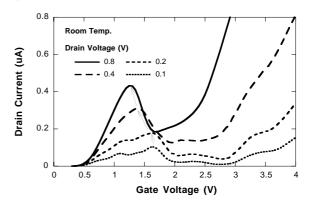


Fig. 6 :  $I_d$ - $V_g$  characteristics at various  $V_{ds}$ . While many peaks are observed at  $V_{ds} = 0.1$  V, only one peak is observed at  $V_{ds} = 0.8$  V.

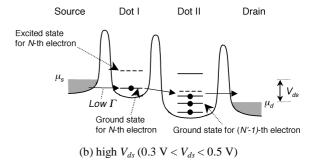


Fig. 7 : Schematic view of the estimated potential profile in this SET at  $V_g$  = 1.6 V for (a) low  $V_{ds}$  and (b) high  $V_{ds}$ . The tunneling rate  $\Gamma$  of electrons from the source to the ground state in the dot I decreases as  $V_{ds}$  is increased. Coulomb staircase will appear when  $V_{ds}$  is further increased and the ground state for (N'-I)-th electron in the dot II is above  $\mu_d$ .