Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 332-333

E-6-5

Analysis of Back-Gate Voltage Dependence of Threshold Voltage of Thin SOI MOSFET and Its Application to Si Single-Electron Transistor

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1. Introduction

To control the characteristics of nano-devices it is important to know their quantum-mechanical electronic states and structural parameters. Threshold voltage (V_{th}) is one of the important probes to reveal the electronic states. From V_{th} itself, we can estimate the energy level of ultra-thin SOI MOSFETs [1] and Si-SETs [2]. On the other hand, we can derive the ratio of effective gate and back-gate capacitances ($C_{G,eff}$ and $C_{BG,eff}$) from the slope of the back-gate voltage (V_{BG}) dependence of V_{th}. Because the ratio is determined not only by structural parameters, such as the gate-oxide (GOX) and the buried-oxide (BOX) thicknesses (t_{ox} and t_{box}), but also by the wave functions of carriers in Si regions, we can obtain information about the structural parameters and positions of carriers from the slope.

In this paper, we report the results of an analysis of the V_{BG} dependence of the V_{th} of thin SOI MOSFETs and peak voltage (V_{peak}, defined as the gate voltage (V_G) giving a drain current peak) of Si SETs. We show that t_{ox} and SOI layer thickness (t_s) of SOI MOSFETs can be evaluated precisely and that the change in the average position of electrons in an island of a SET can be detected even though the island size is of order of 10 nm.

2. Measured Devices and Analysis Method

The devices measured were n- and p-channel thin SOI MOSFETs (Channel lengths and widths were 14 μm and 30 μm, respectively) and n-channel SETs. All devices are fabricated using p-Si SOI wafers. Si SETs were fabricated by PADOX [3], and device structure is the same as that in [2].

The analysis of the measured dependence of the V_{th} on V_{BG} is based on a calculation in which V_{th} is obtained by solving the coupled Poisson and Schrödinger equations using the following trial function as the ground-state function (Considering only the ground state is enough at low temperatures):

$$\Psi(z) = A(\alpha)\sin(\pi z/t_s)\exp(-\alpha z/2), \qquad (1)$$

where z is the distance of an electron in an SOI layer from the interface between GOX and SOI, α is a variational parameter and $A(\alpha)$ is a normalization constant.

3. Results and Discussion

Figure 1 shows the measured and calculated V_{th} as a function of V_{BG} for n- and p-channel SOI MOSFETs at temperature T of 25 K. The parameters used for calculation are shown in the figure, which are consistent with the experimental ones. From Fig. 1, we can see that calculated data agree well with the measured data and that the slopes differ according to the polarity of V_{BG}. This is because t_{ox} increases effectively for positive V_{BG} since electrons localize near the interface between SOI and BOX for n-channel SOI MOSFETs as shown in the inset. The amount of the increase of t_{ox} is approximately given by ($\varepsilon_{ox}/\varepsilon_s$)$\Delta t_s$, where ε_{ox} and ε_s are permittivities of SiO_2 and Si, and Δt_s is the average distance of electrons from the interface between GOX and SOI. On the other hand, t_{box} increases effectively for negative V_{BG} by almost the same amount but hardly has influence because $\Delta t_s << t_{box}$ in this case.

Figures 2 and 3 show the calculated V_{th} and the slope dV_{th}/dV_{BG} as a function of V_{BG} with t_{ox} and t_s as parameters. It can be seen that for n-channel (p-channel) SOI MOSFETs t_{ox} can be determined precisely using the slope in negative (positive) V_{BG} and that t_s can be estimated by that in positive (negative) V_{BG}, once t_{ox} is determined.

The slope can be well described by the following approximated equation (Results calculated by this equation are also shown in Fig. 3, but they almost coincide with the original ones):

$$\frac{dV_{th}}{dV_{BG}} = -\frac{C_{BG,eff}}{C_{G,eff}} = -\frac{(t_s - \langle\beta\rangle)\varepsilon_{ox} + t_{ox}\varepsilon_s}{\langle\beta\rangle\varepsilon_{ox} + t_{box}\varepsilon_s + \varepsilon_{ox}\varepsilon_s / C_{sub}}, \qquad (2)$$

where $<\beta>$ is the average distance of electrons in SOI from the interface between BOX and SOI calculated using Eq. (1) and C_{sub} is the capacitance of p-Si substrate. Equation (2) is derived assuming that a δ-function-like charge sheet exists at $z=t_s-<\beta>$ in SOI. The slope around V_{BG} of 0 V changes largely because p-Si substrate changes between inversion and accumulation in this region. Except around V_{BG} of 0 V, C_{sub} is very large and the third term in the denominator can be omitted.

Because V_{peak} of SETs can be analyzed using a model based on the V_{th} of a SOI MOSFET [2], we can estimate $<\beta>$ of electrons in the island of a SET from the slope of dV_{peak}/dV_{BG} using Eq. (2) by replacing dV_{th}/dV_{BG} with dV_{peak}/dV_{BG}.

Figure 4 shows V_G dependence of drain current of SET at T=25 K with V_{BG} as a parameter. Figure 5 shows V_{peak} as a function of V_{BG} with peak number N as a parameter. In Fig. 5, solid lines are linearly fitted using measured data of 20 V-100 V, except N=3. For N=3, the slope of high V_{BG} (solid line) clearly changes from that of low V_{BG} (dashed line), which probably indicates that the configuration of electrons in Si island changes.

Figure 6 shows dV_{peak}/dV_{BG} as a function of peak number N. The right-side axis is $<\beta>$ calculated using Eq. (2) without C_{sub} and assuming t_{ox}=3.5 nm and t_s=7.5 nm.

It can be clearly seen that the average position of electrons in the Si island changes in a few-electron regime and tends to saturate as the number of electrons increases.

4. Conclusions

The back-gate voltage dependence of threshold voltage was analyzed for thin SOI MOSFETs. The slope is found to be modulated largely not only by the structural parameters but also by the wave functions of carriers, from which the structural parameters can be determined precisely. Moreover, from the back-gate voltage dependence of peak voltages of SET, the average position of electrons in a Si island is shown to change, especially in a few-electron regime, which opens a new way to probe the quantum-mechanical electronic states in the island of SETs.

References

[1] Y. Omura et al., IEEE Electron Devices Lett., **14**, 569(1993).
[2] A. Fujiwara et al., Jpn. J. Appl. Phys. **42**, 2429 (2003).
[3] Y. Takahashi et al., IEEE Trans. ED **43**, 1213 (1996).

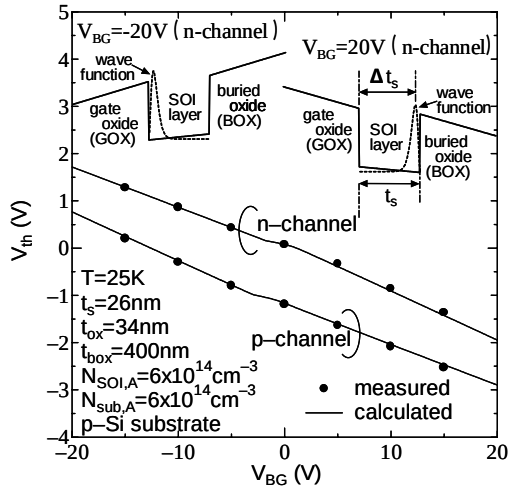

Fig. 1. Measured and calculated V_{th} as a function of V_{BG} for n- and p-channel thin SOI MOSFETs. The measured V_{th}'s are defined as V_G of drain current of $1x10^{-8}$ A. The insets are calculated band diagrams and wave functions around the SOI layer. $N_{SOI,A}$ and $N_{sub,A}$ are acceptor impurity densities in the SOI and substrate.

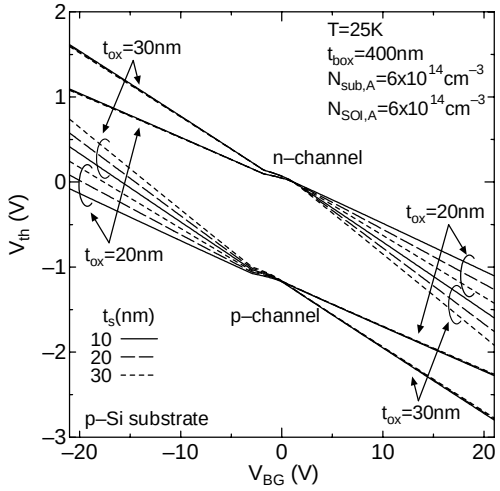

Fig. 2. Calculated V_{th} as a function of V_{BG} for n- and p-channel thin SOI MOSFETs with t_{ox} and t_s as parameters.

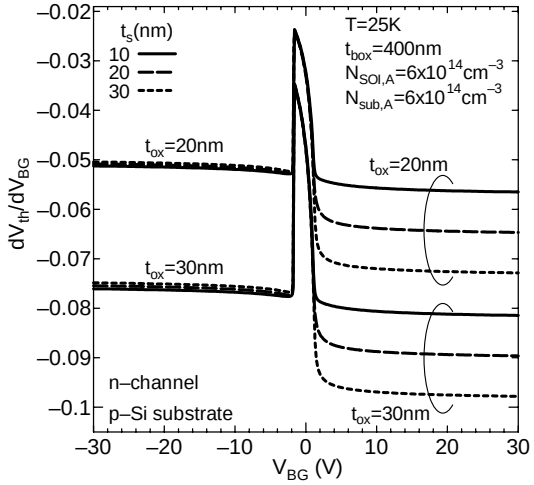

Fig. 3. Calculated dV_{th}/dV_{BG} as a function of V_{BG} for n-channel thin SOI MOSFETs with t_{ox} and t_s as parameters. Calculated data using Eq. (2) are also shown, but almost coincide with original ones using Eq. (1).

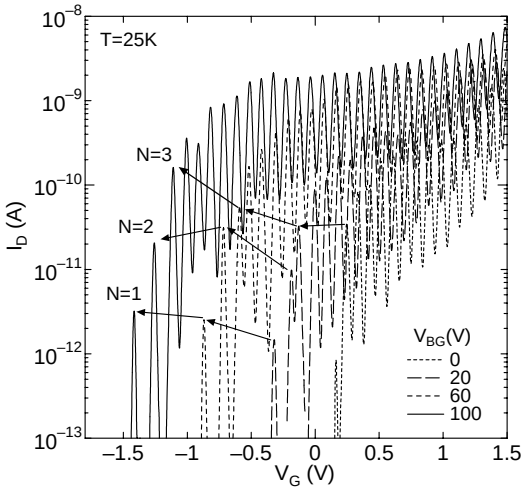

Fig. 4. Measured V_G dependence of drain current I_D for a SET with V_{BG} as a parameter. N is a peak number.

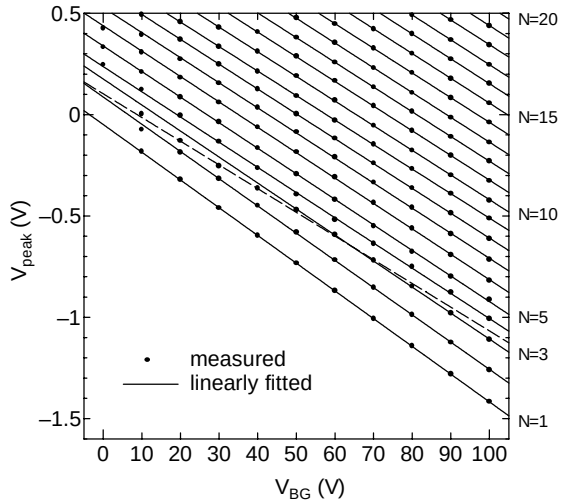

Fig. 5. Measured V_{peak} as a function of V_{BG} for a SET and linearly fitted lines with peak number N as a parameter.

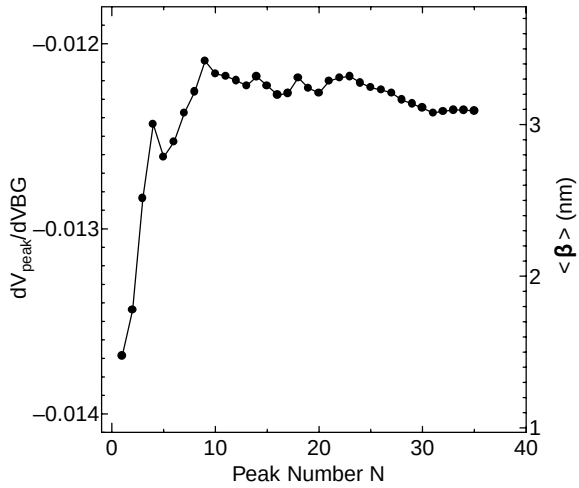

Fig. 6. Measured dV_{peak}/dV_{BG} as a function of peak number for a SET. Right-hand axis is <β>.