

Top-Gate Carbon-Nanotube Field-Effect Transistors with Very High Intrinsic Transconductance

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1. Introduction

Carbon-nanotube field-effect transistors (CNTFETs) are expected to have performance greatly exceeding Si-MOSFETs [1,2]. Advances in device structures such as top gates [3,4] and high-k [2,4] dielectrics have gained high extrinsic transconductance. However, intrinsic performances of CNTFETs have been veiled due to low yields and unstable parasitic effects such as contact resistances.

Intrinsic performance of CNTFETs was investigated by using top-gate structures. Top gates, located on CNTs and far away from source and drain electrodes, have ensured the FET operation by carrier-density control [4]. Reliable device fabrication process utilizing high-yield on-wafer chemical vapor deposition (CVD) [5] of CNTs together with contact technology have enabled us to accomplish systematic studies.

Transconductance of our device reaches $8.7\mu\text{S}$ at a drain voltage of -1 V . Intrinsic transconductance is estimated to be $20\mu\text{S}$ ($13000\mu\text{S}/\mu\text{m}$) in consideration of the parasitic resistance. We also found that the parasitic resistance is dominated by the extension parts of CNTs for our devices. We expect that the performance of CNTFETs will advance further by improving CNT quality and optimising the device structures.

2. Experimental

CNTs were grown by CVD [5] from sub-micron Fe catalyst islands on Si/SiO₂ substrates. Source and drain electrodes were defined to surround Fe islands partially as shown in Fig. 1 (a). A limited number of CNTs bridged the $1\text{-}\mu\text{m}$ gap between the source and drain electrodes as shown in Fig. 1 (b). Gate electrodes were located on CNTs with a gate length of 210 nm on CNTs in between the source-drain gaps. The gate dielectric is very thin (2–3 nm) TiO₂ with high dielectric constant (40-90).

3. Results and Discussion

Drain current I_D depends on drain voltage V_{DS} almost linearly and reaches $8\mu\text{A}$ at $V_{DS} = -1\text{ V}$ as shown in Fig. 2 (a) for a CNTFET with a CNT diameter of 1.5 nm. Drain current I_D is suppressed as gate voltage V_G increases, similar to p -type depletion-mode FETs. The transconductance $g_m = \Delta I_D / \Delta V_G$ is $8.7\mu\text{S}$ for $V_{DS} = -1\text{ V}$ as shown in Fig. 2 (b). Apparent transconductance per unit channel width is

$5800\mu\text{S}/\mu\text{m}$ by assuming the CNT diameter (1.5 nm) as the channel width, about one order as high as those of state-of-art Si-MOSFETs. The parasitic resistance R_p of the device is $130\text{ k}\Omega$, obtained from the I_D saturation observed for $V_G \leq -0.6\text{ V}$. From R_p , intrinsic transconductance is estimated as $g_m^i = g_m / (1 - g_m R_p / 2) = 20\mu\text{S}$ per tube ($13000\mu\text{S}/\mu\text{m}$), which expresses a remarkably high value.

Drain current I_D at $V_{DS} = -100\text{ mV}$ as a function of V_G for different CNTFETs is shown in Fig. 3 (a). Scaling plot indicates that all samples show an identical tendency except for the scaling factor [Fig. 3 (b)]. Figure 3 (c) shows the CNT diameter dependence of $1/R_p$, g_m , and g_m^i . Both g_m and g_m^i change in conjunction with $1/R_p$, consistent with the scaling plot.

Figure 3 (d) shows R_p as a function of $1/g_m$ and of $1/g_m^i$, indicating a linear relation. The parasitic resistance is the sum of contact resistance, R_{contact} , and the CNT resistance at the extension parts between the gate and source/drain, $R_{\text{extension}}$, i.e., $R_p = R_{\text{contact}} + R_{\text{extension}}$. As $R_{\text{extension}} \propto 1/\mu$ and $g_m^i \propto \mu$, where μ is CNT mobility, thus the relation $R_p = R_{\text{contact}} + A/g_m^i$, where A is a constant, should be satisfied. It is concluded from Fig. 3 (d) that the contribution of $R_{\text{extension}}$ to R_p is larger than R_{contact} . The extension resistance can be decreased by improving the quality of CNTs and by decreasing the distances between the gate and source/drain electrodes.

Conclusion

Intrinsic performance of CNTFETs was investigated by using top-gate structures. Intrinsic transconductance is estimated to be $20\mu\text{S}$ ($13000\mu\text{S}/\mu\text{m}$), which is a remarkably high value. Parasitic resistance is dominated by the extension parts for our devices. We expect that the performance of CNTFETs will advance further by improving the CNT quality and optimising the device structures.

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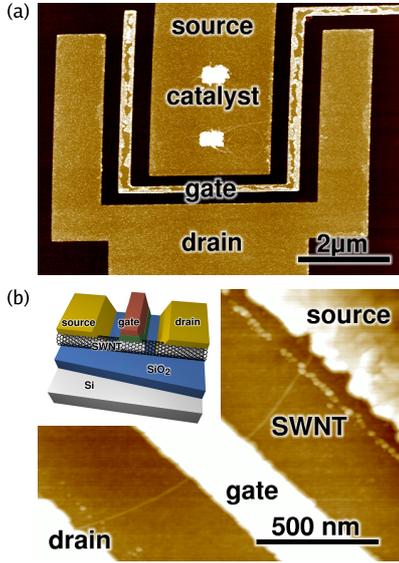


Figure 1: (a) An AFM image of a top-gate CNTFET. (b) An AFM image of a CNT spanning the gap between the source and drain. Inset: schematic structure of the CNTFET.

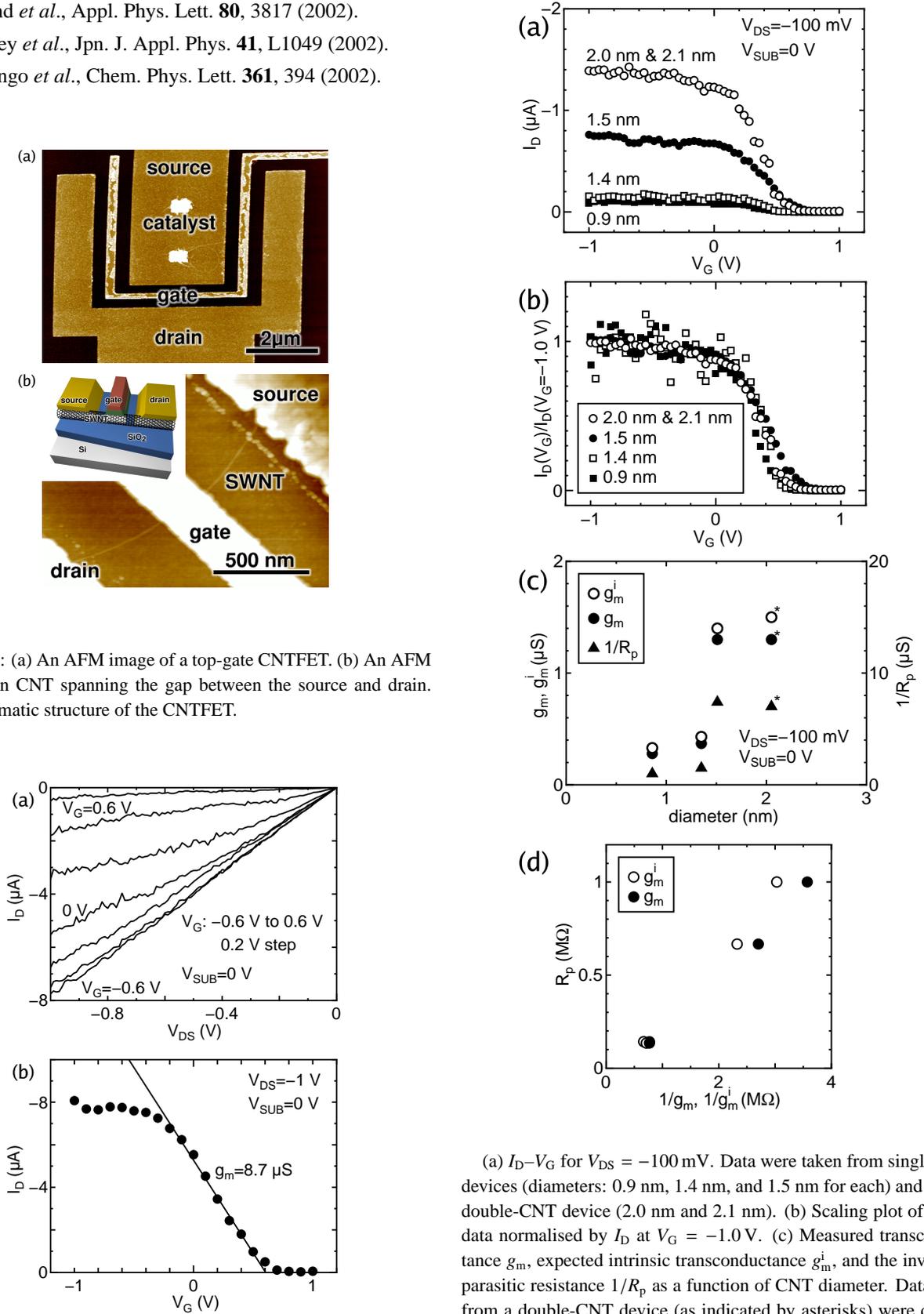


Figure 2: (a) I_D as a function of V_{DS} for a CNTFET with a CNT diameter of 1.5 nm. (b) I_D as a function of V_G for $V_{DS} = -1$ V.

(a) I_D - V_G for $V_{DS} = -100$ mV. Data were taken from single-CNT devices (diameters: 0.9 nm, 1.4 nm, and 1.5 nm for each) and from a double-CNT device (2.0 nm and 2.1 nm). (b) Scaling plot of I_D - V_G data normalised by I_D at $V_G = -1.0$ V. (c) Measured transconductance g_m , expected intrinsic transconductance g_m^i , and the inverse of parasitic resistance $1/R_p$ as a function of CNT diameter. Data taken from a double-CNT device (as indicated by asterisks) were divided by a factor of 2. (d) R_p as a function of $1/g_m$ and $1/g_m^i$.