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Hybrid Silicon Nanocrystal Silicon Nitride Memory

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Abstract

This paper introduces a new non-volatile memory device using silicon nanocrystals embedded between tunnel oxide and silicon nitride storage layers. This hybrid device programs at lower voltages than a conventional SONOS memory cell and has a larger threshold voltage shift than Si nanocrystal memories. Electrical data from MOSFETs and MOS capacitors are used to illustrate the differences between SONOS, Si nanocrystal, and hybrid memory device architectures. Program and erase measurements show that the hybrid memory device results in program/erase times that are reduced by two orders of magnitude when compared to SONOS with only a small impact on data retention.

Introduction

Thin film storage devices such as SONOS [1] and Si nanocrystal floating gate memories [2] are desirable medium to low voltage alternatives to conventional floating gate (FG) [3] memories because of lower cost of integration, particularly in embedded applications, and resistance to charge loss due to tunnel oxide defects. However, both have their limitations. SONOS requires a high program and erase voltage (+- 10-12V) because of the need to Fowler-Nordheim tunnel into the nitride traps. Nanocrystal memory, which permits direct tunneling into Si nanocrystals, can be programmed at 6-8V for 35-40 Å tunnel oxide. [4] But at these voltages, Coulomb blockade effects may prevent the large threshold voltage shift (3-5V) associated with SONOS devices which makes nanocrystal memories susceptible to threshold voltage variation. An ideal non-volatile memory device would achieve high threshold voltage shifts using low program voltages.

The Hybrid Structure and Principle

Figure 1 shows the hybrid memory architecture. This device is comprised of a thin tunnel oxide, a layer of Si nanocrystals and a thick nitride layer on top of which is the control dielectric. A variant of this device have been proposed by Yamazaki [5] in order to improve SONOS data retention. The presence of the nanocrystal facilitates tunneling of charge (electrons or holes) into the nitride layer by providing intermediate states, resulting in increased charge tunneling into the nitride at low voltages compared to SONOS.

Results and Discussion

MOS capacitors and MOSFETs were fabricated to illustrate the effects discussed. Silicon nanocrystals were deposited using a CVD technique, the nitride was a furnace nitride and the control oxide was high temperature oxide for the MOS capacitors and steam oxide for the MOSFETs. Figure 2 shows a plan view SEM of silicon nanocrystals where a density of nearly 10^{12} cm^{-2} has been obtained and Figure 3 shows an energy filtered TEM highlighting crystalline Si nanocrystals about 5nm in size in a hybrid transistor. Figure 4 compares the threshold voltage shifts obtained using MOS capacitors for SONOS, nanocrystal memory and hybrid device configurations at PROGRAM and ERASE voltages of +/- 4V respectively after about 100 seconds. This very low program/erase voltage dramatically demonstrates the differences between the three devices. The tunnel oxide/nitride/control oxide thicknesses were 30Å/90Å/50Å. The voltage shifts for the SONOS, nanocrystal memory and hybrid device are 100mV, 500 mV and 3V respectively. Silicon nanocrystals embedded in the hybrid device greatly facilitate the transfer of charge to the nitride resulting in a much higher threshold voltage. Figure 5 shows the corresponding program and erase (P/E) curves. Almost all the P/E in the nanocrystal memory occurs in less than 1 second and subsequent charge transfer is possibly impeded by Coulomb blockade [2]. The hybrid device continues to charge at an appreciable rate even after 100 seconds. Figure 6 shows the corresponding program and erases curves for SONOS and hybrid device MOSFETs (10x0.15 um) with 22 Å tunnel oxide and similar control oxide and nitride layers to the MOSCAP devices. At low program and erase voltages (+/-4V, +/- 6 V) a two order of magnitude increase in program and erase speeds is seen using a hybrid device versus a SONOS device. At higher voltages (+/- 10 V) differences in speed between SONOS and hybrid devices decrease due to the increased role of modified Fowler-Nordheim tunneling in charge transport to the nitride.

Figure 7 compares the short-term data retention (<1000 sec) between a SONOS and hybrid MOSFET charged to the same threshold voltages. The decay in threshold voltage for both program and erase threshold voltages is comparable on this time scale. A longer term data retention measurement for a hybrid MOS capacitor with the same film stack is shown in Figure 8. This figure also includes a comparison of the charge retention measurements to calculations of charge loss assuming that the capacitor loses charge equivalent to a SONOS device with a 16 Å tunnel oxide. The charge loss is well described by a SONOS model even though the model does not account for concomitant charge loss by the nanocrystals. Data retention at long times is determined by charge stored in the nitride layer and the transport of charges from trap-to-trap in the nitride. Hence the difference between the estimated tunnel oxide thickness for retention and the physical thickness is not expected to affect charge storage.

Conclusions

This paper presents a new hybrid Si nanocrystal/SONOS type memory bit that can be used for embedded memory applications. This memory bit uses a layer of Si nanocrystals between the SONOS storage nitride and the tunnel oxide that facilitates the transfer of charge to the nitride. Measurements of program and erase time show up to a two order of magnitude decrease in program speed for the hybrid device compared to SONOS at low voltages. Data retention for the devices is comparable to SONOS devices with a thinner tunnel oxide. The lower voltage of operation compared to SONOS along with a simple integration into a standard CMOS flow makes it an attractive candidate for use in embedded memory applications.

References

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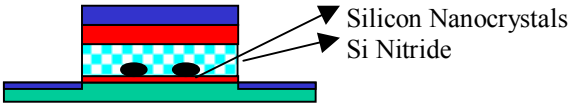

Figure 1: Hybrid Si nanocluster/SONOS bit

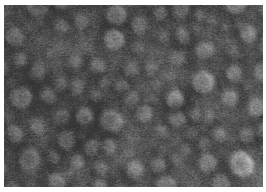

Figure 2: Plan view SEM showing Si nanocrystals on oxide

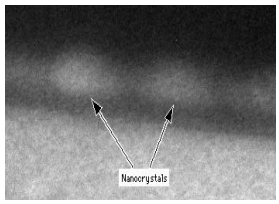

Figure 3: Energy Filtered TEM showing nanocrystals in hybrid device transistor

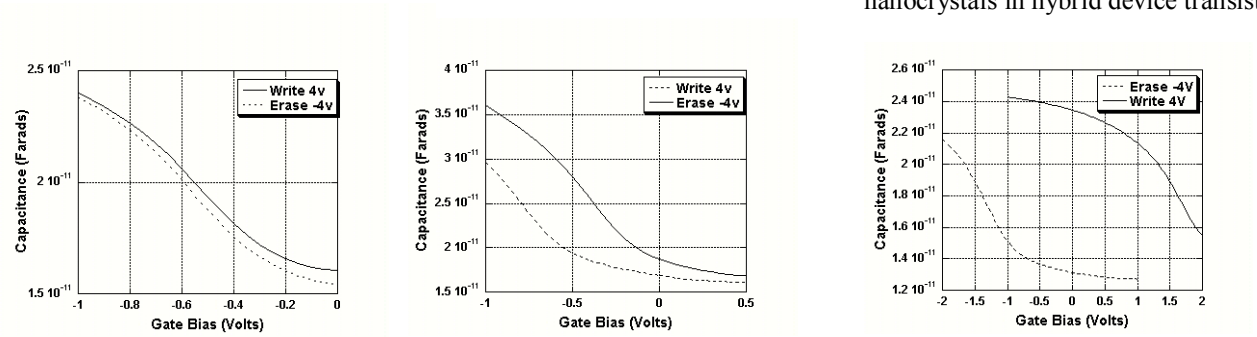

Figure 4: Memory effect measured as a voltage shift for SONOS (left), nanocrystal memory (middle) and hybrid (right).

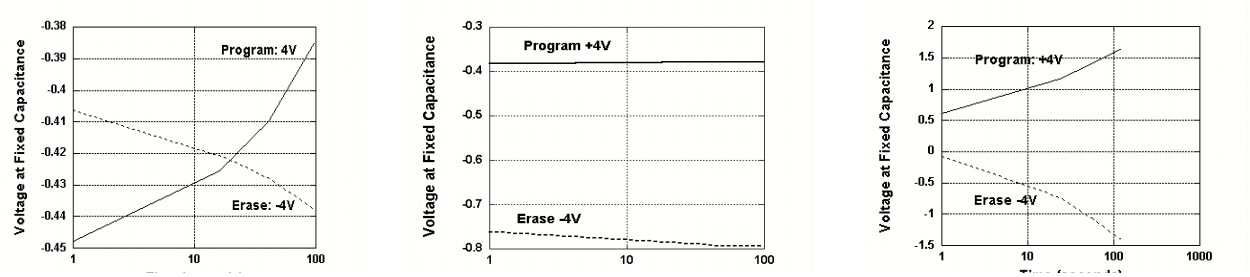

Figure 5: Low voltage P/E characteristics of SONOS (left), nanocrystal memory (middle) and hybrid (right)

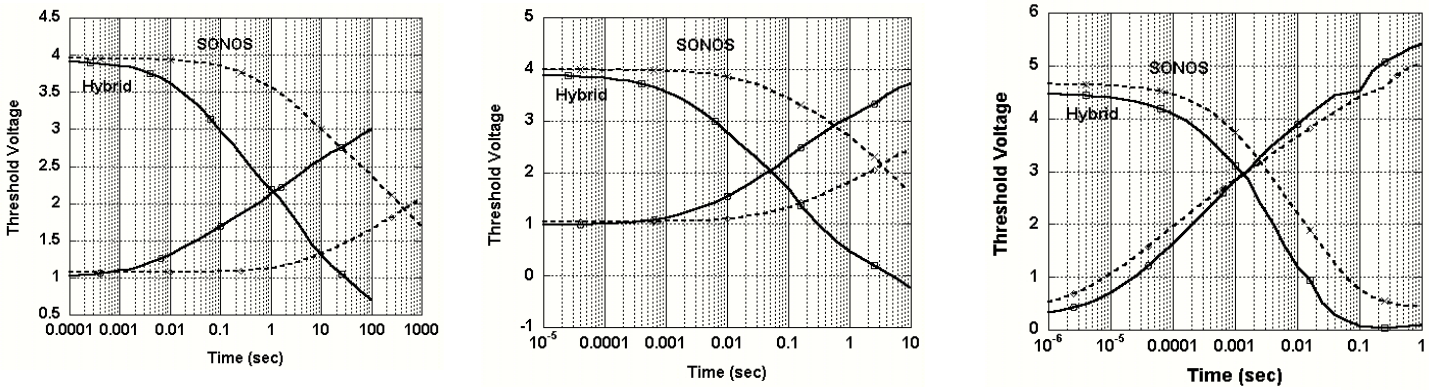

Figure 6: SONOS and Hybrid P/E characteristics at +/-4V (left), +/- 6 V (middle) and +/-10 V (right)

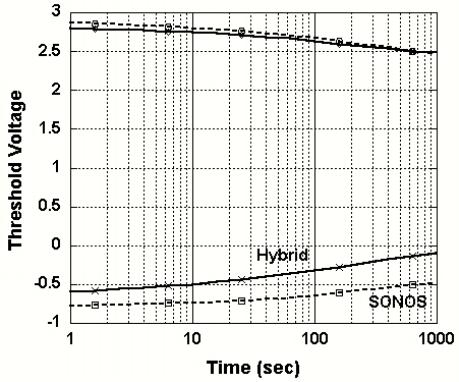

Figure 7: SONOS and Hybrid MOSFET Data Retention

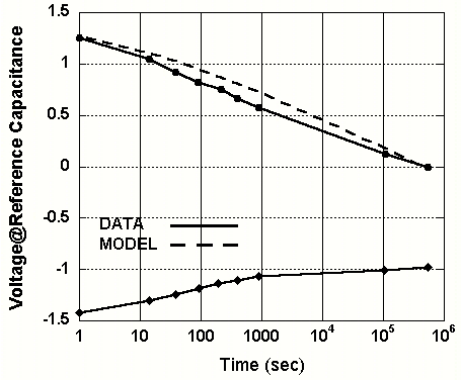

Figure 8: Longer Term Hybrid MOSCAP Data Retention