Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 850-851

E-9-3

Monte-Carlo Simulation of Single-Electron Nanocrystal Memories

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1. Introduction

Nanocrystal memory is one of the promising candidates for the future solid-state storage devices, and considered to be appropriate for the low voltage and low power application.

Until now, however, the researchers in this field concentrated more on the fabrication of them than on the modeling or simulation for theoretical analysis [1-3]. Even if there were a few modeling and simulation studies, their scope was limited to a detailed analysis on the single charging/discharging or quantum confinement phenomenon itself in one nanocrystal quantum dot, under the assumption that the interaction between the neighboring dots could be ignored [4-5]. In addition, there has not been a concrete research about extracting the realistically measurable values such as drain currents or threshold voltages, out of the states of many quantum dots and physical dimensions of nanocrystal memories.

On these backgrounds, we present our Monte-Carlo simulation results about programming characteristics of nanocrystal memories including the interactions of many quantum dots. We modeled the nanocrystal memory as a network of a number of single tunnel junctions and channel resistances. From this simulation, we can understand better the programming operation mechanism of nanocrystal memories, and present the rules that should be considered for the design of single electron nanocystal memories.

2. Modeling of Nanocrystal Memory Devices

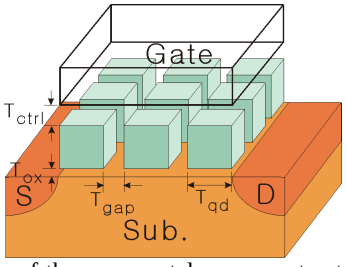


Fig.1 Schematic of the nanocrystal memory structure used in this simulation work. The actual number of the dots is 10X10.

- Device Structure and Parameters

Fig.1 shows the device structure considered in this work. The actual number of quantum dots used in the simulation is 10 X 10 = 100, not 3 X 3. Each dot is assumed to have cubic form, regular size and spacing. In the figure, T_{ox} is the tunneling oxide thickness between channel and dot, T_{ctrl} is the control oxide thickness between gate and dot, T_{gap} is the distance between neighboring dots, and T_{qd} is the corner length of a cubic quantum dot. Channel and dots are assumed to be composed of Si.

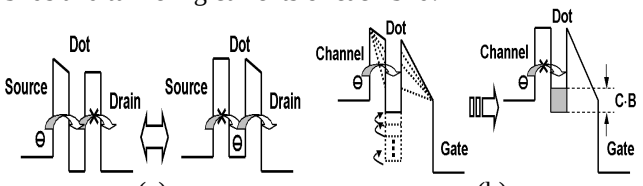
- Single Tunnel Junctions

According to the assumptions of orthodox theory [6], the energy quantization in quantum dots is ignored, and the tunneling rate Γ of STJs(single tunnel junctions) can be expressed as,

$$\Gamma = \frac{-\Delta F}{e^2 R_t [1-\exp(\Delta F / k_B T)]}, \qquad (1)$$

where ΔF is the total system energy difference before and after the tunneling event, and tunneling resistance R_t is the factor which is determinable from the shape of the tunneling barrier or empirically from the I-V relation of the tunnel junction. R_t is often regarded as a constant at a fixed bias condition.

In the case of single electron transistors, this R_t is almost constant at a given bias condition because the quantum dot alternates mainly between the neighboring two states (Fig.2 (a)) [7]. But for the single electron memory, the successive charging in quantum dots changes the shape of tunneling barriers significantly (Fig.2 (b)), and we cannot treat R_t as a constant any more. So, we modified every STJs' R_t as tunneling occurs, by calculating the electric field on the STJs and tunneling currents of each STJ.



(a) (b)

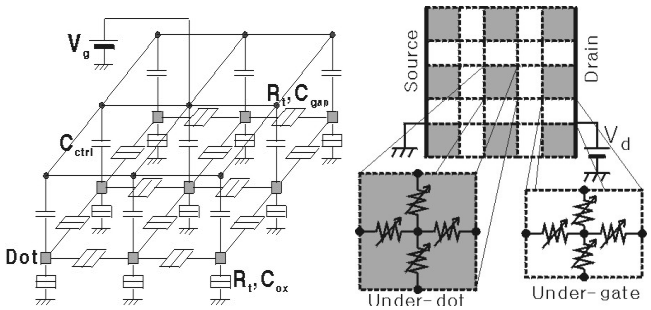
Fig.2 Change of band diagram : (a) SET during on-state (b) SEM during programming, eventually arriving at Coulomb Blockade condition.

- Network of STJs

We cannot exclude the probability of inter-dot tunneling, and STJs were introduced between the neighboring quantum dots, as well as between the quantum dot and the channel. During programming, the source, drain and substrate were grounded, and the nanocrystal memory was modeled as a network of STJs as in Fig.3 (a).

- Calculation of I_d or V_{th}

The channel current and threshold voltage could be obtained by modeling the channel as a resistance network controlled by the gate and quantum dot potentials. We partitioned the channel area into the region just under the quantum dots and the region under the gate which is not screened by the quantum dots, as in Fig.3 (b). And then, each block of channel was simplified as a combination of four small variable resistors.



(a) (b)

Fig.3 (a) Equivalent STJ circuit for a nanocrystal memory during program operation (b) Channel modeling of the nanocrystal memory for extracting drain current and threshold voltage.

3. Simulation Results and Discussions

In general, we followed well-known procedure for the Monte-Carlo simulation of STJ circuits [8]. For the simulation of static programming characteristics, we assumed that the temperature T is 0K and program duration time is long enough to reach Coulomb Blockade condition. According to Fig.4, there is always gradual domain between plateaus. If T_{gap} is large enough and the effect by neighboring dots lessens, each dot has nearly independent property, so the average number of electrons in each dot shows a sharp step-like programming characteristic. But the transition region enlarges as the nanocrystal dots come closer, and the characteristics resemble those of conventional flash memory. This is contradictory to the general belief that perfectly regular and uniform nanocrystal dots enable the ideally sharp step-like programming characteristics from single-electron effect [9].

Dot size influence on the programming characteristics was shown in Fig.5. As is generally known, the threshold voltage shift for another electron in quantum dot increases as the dot size becomes smaller. In Fig. 6, as explained before, the plateau region in step-like features enlarges when the inter-dot distance is large. But the threshold voltage shift decreases, because the channel region controlled by the quantum dots shrinks.

As the programming time is always limited in real situation, we must include timing factor in considering realistic nanocrystal memory. Fig.7 shows the programming characteristics at different program pulse duration T_p. When T_p is long enough, the shape of curves resembles that of the static case in Fig.4, but the shape is destroyed as T_p decreases. Thus, a considerable duration of program pulse is required to observe the single electron charging effect in nanocrystal memories.

4. Conclusions

We established a simulation technique to predict the nanocrystal memory characteristics considering various device parameters, by combining Monte-Carlo simulation of STJs' network and channel resistance modeling. From the results, nanocrystal memory parameters, such as dot size and spacing between dots, are closely related to programming characteristics. The presented simulation techniques and the results could be a good reference for designing single-electron nanocrystal memories in the future.

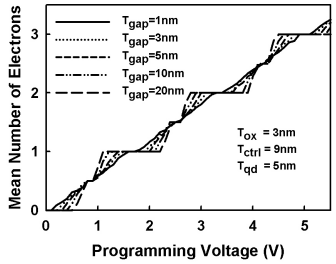


Fig.4 Mean number of electrons in all the nanocrystal dots as a function of programming voltage

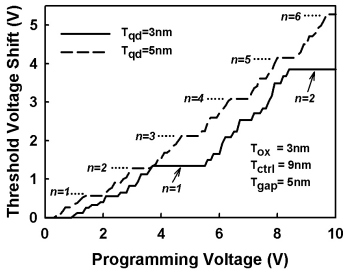


Fig.5 Quantum dot size dependence of the programming characteristics

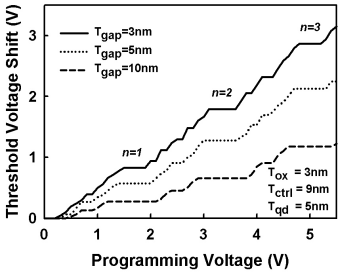


Fig.6 The influence of the gap between the dots on the programming characteristics of the nanocrystal memory

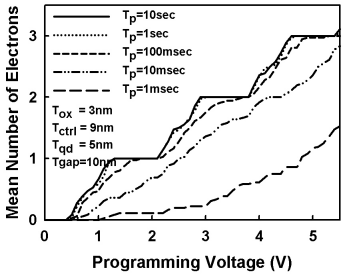


Fig.7 Programming characteristics of the nanocrystal memory as a function of program pulse duration

Acknowledgements

This work was supported by the Terabit-level Nano Device project as a part of 21st Century Frontier Program.

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