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Ultrahigh Performance InP HEMTs

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1. Introduction

InP-based high electron mobility transistors (HEMTs) show excellent high-frequency performance because of their high electron mobilities, high electron velocities, and high sheet electron densities. In our previous works, we developed several fabrication techniques [1-4] and fabricated $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ lattice-matched (L-M-, x=0.53) and pseudomorphic (P-, x=0.7) HEMTs with decananometer-scale gate length L_g. In this paper, we review our recent results for InP-based HEMTs.

2. Fabrication Process and Device Performance

L-M- and P-HEMT epitaxial layers were grown on semi-insulating (100) InP substrates by metal organic chemical vapor deposition. The L-M-HEMT layers, from bottom to top, consist of a 300-nm InAlAs buffer, a 15-nm InGaAs channel, a 3-nm InAlAs spacer, a Si-δ-doped sheet (5×10^{12} cm^{-2}), a 10-nm InAlAs barrier, a 6-nm InP, and a 30-nm Si-doped InGaAs cap (1×10^{19} cm^{-3}) layer. In the P-HEMT, the $In_{0.7}Ga_{0.3}As$ channel layer is 12-nm thick and the $In_{0.53}Ga_{0.47}As$ cap layer is 40-nm thick. The other layers are the same as those in the L-M-HEMTs. T-shaped Ti/Pt/Au Schottky gates with widths W_g of 50×2 µm were fabricated using electron beam lithography and a standard lift-off technique within a source-drain spacing L_{sd} of 2 µm. A two-step-recessed gate technique [5] was used to reduce the gate-channel distance d while maintaining a high electron sheet density in the side-etched region of the gate-recess.

S-parameters were measured at frequencies up to 50 GHz. Note that the parasitic capacitance due to the probing pads was subtracted from the measured S-parameters. Figure 1 shows the gate-channel distance d dependence of f_T for the 25-nm-gate L-M-HEMTs under a drain-source voltage V_{ds} of 0.8 V. As clearly seen in Fig. 1, the f_T increases with a decrease in d. By decreasing the d from 15 to 4 nm, the f_T was increased from 377 to 500 GHz [3]. Figure 2 shows the gate-channel distance d dependence of transconductance g_m and gate capacitance C_g for the HEMT in Fig. 1. The g_m increased much more with a decrease in the d than the C_g did. Thus, reducing the gate-channel distance increases the f_T, which results from an increase in the g_m. Increasing the In content in the InGaAs channel layer (P-HEMT) is effective in increasing the f_T, because the electron effective mass in the InGaAs layer becomes lighter by increasing the In content. We obtained an f_T of 562 GHz with a d of 4 nm for P-HEMTs [2].

An asymmetric gate-recess structure with a shorter source-side recess and a longer drain-side recess is effective for obtaining a higher maximum oscillation frequency f_{max}. We developed a simple and high-precision fabrication technique for HEMTs that have an asymmetrically recessed T-shaped gate [4]. The technique uses a conventional triple-layer resist that has additional slit patterns beside a gate-foot pattern in the bottom layer. The gate metal is evaporated at a tilted angle to avoid evaporation through the slit patterns. The source- and

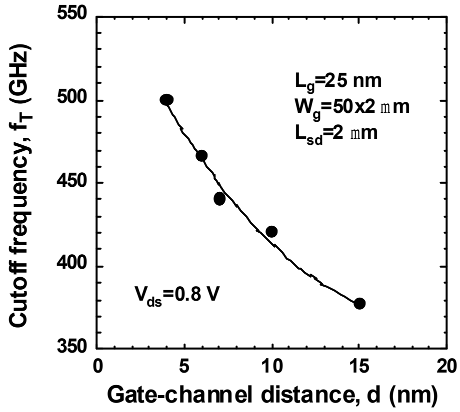

Fig. 1 Gate-channel distance d dependence of the cutoff frequency f_T for the 25-nm-gate L-M-HEMTs.

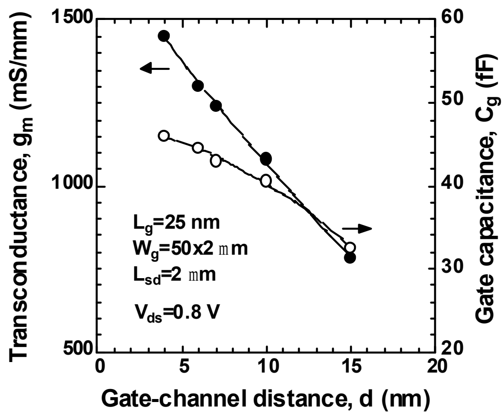

Fig. 2 Gate-channel distance d dependence of the transconductance g_m and gate capacitance C_g for the 25-nm-gate L-M-HEMTs.

drain-side recess length (L_{rs}, L_{rd}) can be precisely controlled by the etching time and by the size and position of the slits. We used P-HEMT with a 20-nm InGaAs cap layer for this process. Figure 3(a) shows a bird's-eye view scanning electron microscopy (SEM) image of a triple-layer resist with additional small slit patterns after recess etching with an L_g of 60 nm. The recess etching was successfully done through such very small slits. The Ti/Pt/Au gate metal was evaporated at a tilted angle of 45°. Figure 3(b) shows a cross-sectional SEM image of a complete T-shaped gate with an L_g of 60 nm, an L_{rs} of 80 nm, and an L_{rd} of 190 nm.

Figure 4 shows the frequency dependence of current gain $|h_{21}|^2$ and Mason's unilateral power gain U_g of 60-nm-gate P-HEMTs that have a symmetric [L_{rs}=L_{rd}=80 nm (a)] and an asymmetric recess [L_{rs}=80 nm, L_{rd}=190 nm (b)] under a V_{ds} of 1.0 V and a gate-source voltage V_{gs} of -0.4 V. A slightly lower f_T of 303 GHz was obtained for the asymmetric device than that for the symmetric one (308 GHz). On the other hand, the asymmetric device exhibited a much higher f_{max} of 428 GHz, which is 70% higher than that for the symmetric one (244 GHz). To understand the increase in f_{max}, equivalent circuit elements were extracted from the measured S-parameters. Concerning the g_m, both devices showed almost the same value of ~1.0 S/mm. The drain conductance g_d and the gate-drain capacitance C_{gd} were significantly decreased for the asymmetric device by 40% and 35%, respectively, compared to the symmetric one. Both of which are effective for the higher f_{max}.

3. Summary

In summary, we reviewed our recent results for InP-based HEMTs that have high f_T or high f_{max}. The f_T increases with a decrease in the gate-channel distance d in L-M-HEMTs. We obtained an f_T of 500 GHz for the L-M-HEMT, and an f_T of 562 GHz for the P-HEMT. On the other hand, we succeeded in increasing the f_{max} by using an asymmetrical gate-recess structure with a longer L_{rd}. We will show the latest results at the conference.

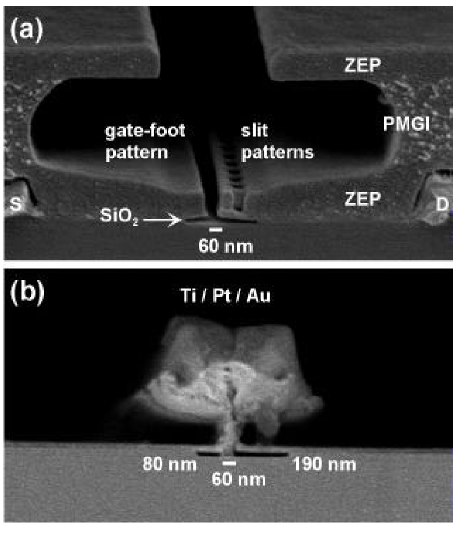

Fig. 3 SEM images of a triple-layer resist with additional small slit patterns after recess etching (a), and a T-shaped gate with an asymmetric recess (b).

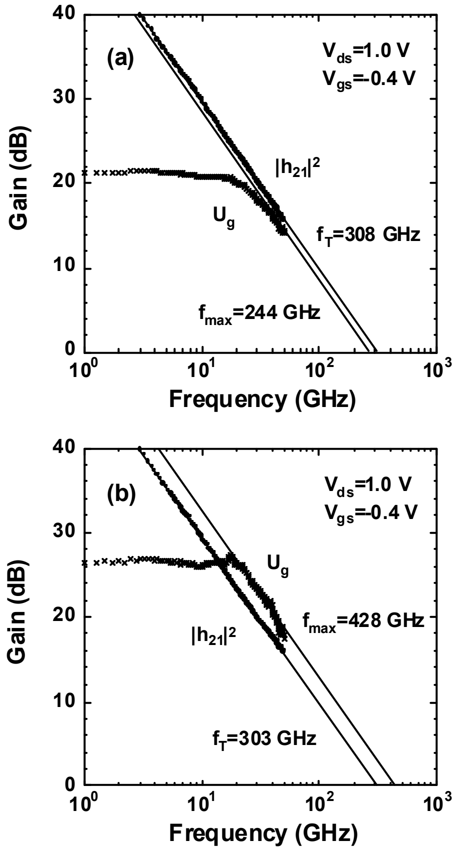

Fig. 4 Frequency dependence of the current gain $|h_{21}|^2$ and Mason's unilateral power gain U_g of 60-nm-gate P-HEMTs with a symmetric recess [L_{rs}=L_{rd}=80 nm (a)] and an asymmetric recess [L_{rs}=80 nm, L_{rd}=190 nm (b)].

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