

High f_T 30nm $\text{In}_{0.7}\text{GaAs}$ HEMT fabricated with $\text{SiO}_2/\text{SiN}_x$ sidewall gate Process and BCB Planarization

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1. Introduction

$\text{InGaAs}/\text{InAlAs}$ HEMT on InP substrate has shown the excellent frequency characteristics due to the enhanced electron mobility and the increased conduction band discontinuity (ΔE_c) [1-2]. Recently, the device microwave characteristics have been improved by reducing the gate length (L_g) to nano-meter scale and adopting the highly strained In_xGaAs channel ($x > 0.53$) [3]. According to the Fujitsu group's work, f_T of 396GHz for the strained $\text{In}_{0.7}\text{GaAs}$ channel HEMT with L_g of 50nm was reported [3].

In this work, the sidewall gate process was developed in order to overcome the lithography limitation. Through the sidewall process, initially defined line length could be lessened to half [4]. To fill the schottky gate metal effectively in narrow line opening with high aspect ratio above 3, the sputtered tungsten (W) was used instead of conventional E-beam evaporated metal. With the developed processes, 30nm $\text{In}_{0.7}\text{GaAs}$ HEMT was fabricated and characterized.

2. 30nm Triple Gate Process

Figure 1 shows the over-all SEM photographs for the sidewall gate process in detail. Through dielectric re-deposition and dielectric etch-back, the final gate length (L_g) could be lessened by the dimension of the two side-wall spacers [4]. The obtained final gate length after the dielectric etch-back was 30nm.

The procedure for the fabrication of triple shaped gate structure is shown in figure 2. After the tungsten sputtering in the sidewall gate, 2nd gate metal (Ti/Au) with 100nm thickness was evaporated and lifted off, and then unnecessary tungsten was removed by RIE. Finally, planarization using BCB dielectric with low dielectric constant (ϵ_r) of 2.8 was carried out and 3rd gate metal (Ti/Au) with 600nm thickness was evaporated and lifted off. Figure 3 shows the SEM photographs of the fabricated 30nm triple shaped gate structures.

3. Characterization of 30nm $\text{In}_{0.7}\text{GaAs}$ HEMT's

Pseudomorphic $\text{InGaAs}/\text{InAlAs}$ HEMT epitaxial layer was grown by a solid-source molecular beam epitaxy (MBE) on a 3 inch semi-insulating InP substrate. Strained 8nm $\text{In}_{0.7}\text{GaAs}$ channel was adopted to enhance the carrier transport properties. The hall measurement results indicated

a 2-DEG density of $3 \times 10^{12}/\text{cm}^2$ with a low field Hall mobility of $10,300\text{cm}^2/\text{V-sec}$ at 300K.

Device fabrication begins with mesa isolation down to the InAlAs buffer layer by wet chemical etching. For S/D ohmic contact, Ni/Ge/Au(10/45/120nm) was evaporated, lifted off and alloyed at 320°C in H_2 ambient. The measured ohmic contact resistance was as small as 0.035 Ω -mm, which is acceptable for sub-50nm gate device. The sidewall gate process was applied to form 30nm gate opening, in which selective gate recess etching with succinic acid was done.

The fabricated devices were characterized through on-wafer measurements for DC and microwave performance analysis. The output I-V transfer curves were plotted in figure 4. The device was found to have V_{th} of -0.3V, I_{dss} of 180mA/mm, $G_{m,max}$ of 1.6S/mm and BV_{gd} of -4V. Up to the drain bias (V_{ds}) of 1.3V, the device has showed little short channel effects such as the abnormal increase of G and the shift of V_h with drain bias. The small-signal S-parameters for 2x50 μm device were measured using on-wafer probing and network analyzer (1~40GHz). Shown in figure 5 was the plot of H_{21} versus the frequency for the device biased near peak $G_{m,max}$ region. Extrapolating H_{21} to zero gain with -6dB/octave slope, the estimation of 421GHz was made for f_T . We believe that these results demonstrated the excellent sub-50nm InGaAs HEMT with a little short channel effect.

4. Conclusions

We have fabricated 30nm $\text{In}_{0.7}\text{GaAs}$ HEMT with triple shaped gate metal using sidewall process and BCB planarization. Fine lines such as 30nm could be obtained by dual $\text{SiO}_2/\text{SiN}_x$ sidewall process and the triple shaped gate metal process assisted by BCB layer did provide the metal structure stability and small parasitics. The developed process was applied to fabricate 30nm InGaAs HEMT's, which led to $G_{m,max}$ of 1.6S/mm and f_T of 421GHz. We demonstrated that 30nm InGaAs HEMT's could be successfully fabricated through reproducible and damage-free sidewall process without the aid of state-of-the-art lithography machine.

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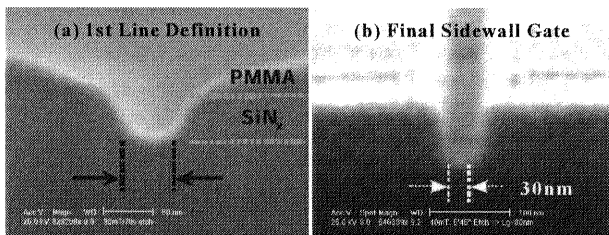


Fig 1. SEM Photographs for 30nm SiO₂/SiN_x Sidewall Process

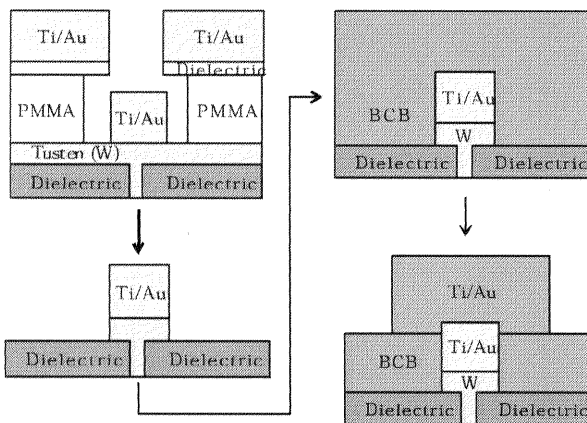


Fig 2. Procedure for BCB Assisted Triple Gate Process

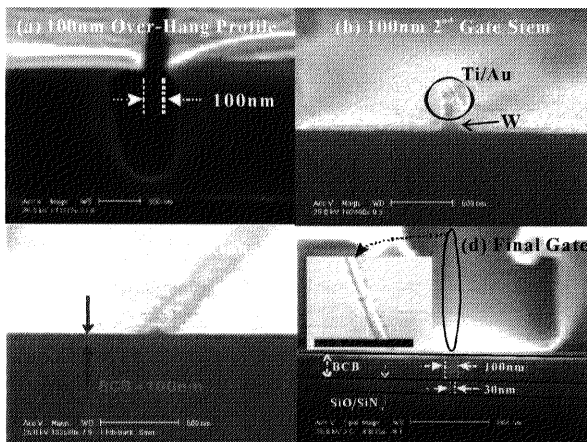
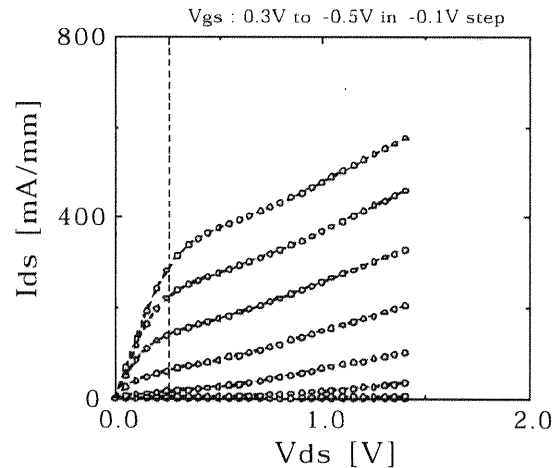
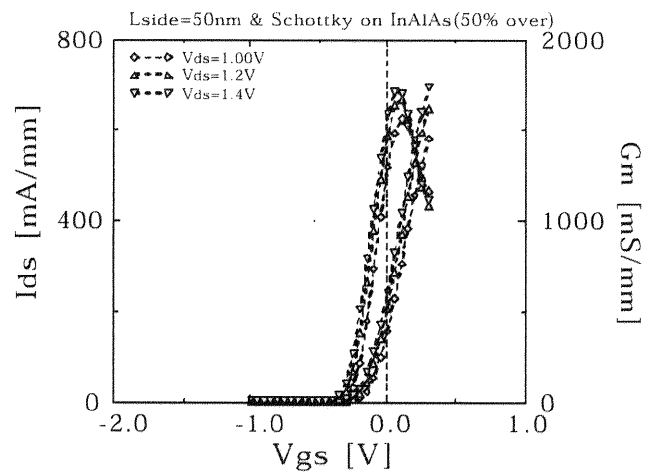


Fig. 3 SEM Photographs for Triple Gate Metal Process



(a) DC I-V Transfer Curve



(b) DC Transconductance Curve

Fig 4. DC characteristics of 30nm HEMT's

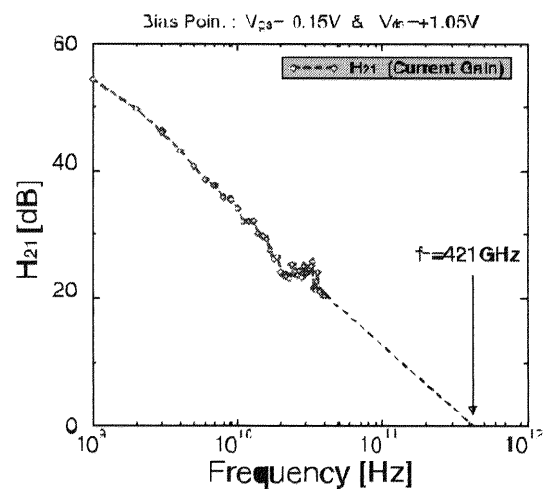


Fig 5. Microwave Performance of 30nm HEMT's