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InP/InGaAs Tunneling Emitter Bipolar Transistor (TEBT)

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1. Introduction

The tunneling emitter bipolar transistor (TEBT), based on a modified HBT structure, was first proposed by Xu et. al. [1-3]. The main feature of a TEBT is the introduction of a very thin tunneling barrier between the n-type emitter and p-type base of a normal HBT structure. Due to the significant difference of tunneling probability for electrons and holes, electrons can be injected by tunneling from the emitter into the base, while the tunneling probability for holes is kept small [4]. Therefore, the emitter injection efficiency is improved. A thicker barrier causes the better suppression of hole injection from base toward emitter and increases the current gain. Yet, a too thick barrier leads to the decreases of current gain due to the decrease of the electron injection current. Chen et. al. reported that a barrier thickness ranged between 50 and 200 Å is beneficial for electron injection and hole localization [5]. The emitter tunneling barrier is also a natural stop layer for wet etching process. The emitter series resistance can be reduced because of the absence of bulk wide-gap emitter. In addition, the emitter size effect of conventional HBTs can be reduced due to the non-equilibrium electron transport.

In this work, we demonstrate an interesting InP/InGaAs TEBT which is based on an HBT structure with a 200Å InP tunneling barrier between the InGaAs emitter and base. Good device properties of the studied InP/InGaAs TEBT are obtained.

2. Experimental

The experimental common-emitter I-V characteristics of the studied TEBT, without passivation structure, at different collector current regimes are shown in Fig. 1. The used emitter size is $50\times50\mu m^2$. Figure 1(a) shows the I-V characteristics at ultra-low collector current regime. The corresponding band diagram of the studied TEBT is depicted in the inset of Fig. 1(a). Under these low collector current levels, the noise performance and relatively high leakage are observed. It is worth to note that even at the collector current of I_C =20nA, a small-signal current gain about 30 is still obtained. The critical requirements for low-power electronics are low operation currents and voltages. Thus, the ultra-low current operation capability of the studied TEBT is beneficial for low-power circuits applications. The I-V characteristics of the studied device at medium collector current regime are shown in Fig. 1(b). The small-signal current gain is 120 at a collector current of I_C =16mA. The common-emitter breakdown voltage BV_{CEO} is higher than 2V. The enlarged I-V characteristic near origin is shown in the inset of Fig. 1(b). Significantly, a very small collector-emitter offset voltage ΔV_{CE} of 40mV is observed. It is believed that the small offset voltage is mainly caused by the negligible turn-on voltage difference between the effective B-E and B-C junctions. In other words, this small ΔV_{CE} shows the negligible geometrical and electrical asymmetries between B-E and B-C junction [6]. This value is comparable or even superior to conventional InP/InGaAs HBTs [7-9]. This small offset voltage can indeed decrease the power consumption and increase the logic swing of output voltage in digital circuit applications. The small-signal current gain is higher than 300 at the collector current of I_C =95mA as shown in Fig. 1(c). Figure 2 shows the measured DC current gain β as a function of collector current I_C. The collector-base voltage is fixed at V_{CB}=0V. The studied device can be operated under extremely wide collector current regimes. The operation regime is wider than 11 decades in magnitude of collector current, i.e., from the collector current of $I_C=10^{-12}$A to $I_C=10^{-1}$A. Experimentally, the studied device exhibits the current gain greater than unity even the collector current is decreased down to pA level. The current gain β about 3 is obtained at an ultra-low collector current of 3.9×10^{-12}A (1.56×10^{-7}A/cm^2). To our knowledge, as compared with previously reported works [10-13], this is

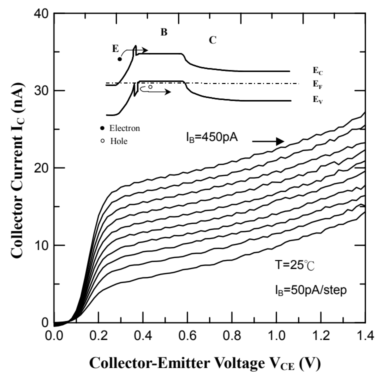

Fig. 1(a) Typical common-emitter I-V characteristics of the studied InP/InGaAs TEBT at ultra-low collector current regimes.

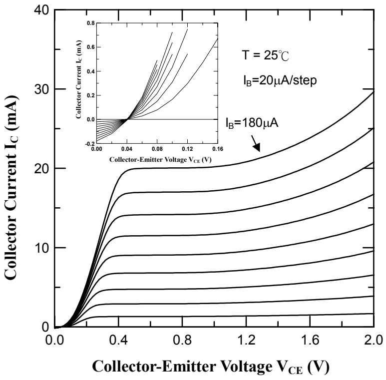

Fig. 1(b) Typical common-emitter I-V characteristics of the studied InP/InGaAs TEBT at medium collector current regimes.

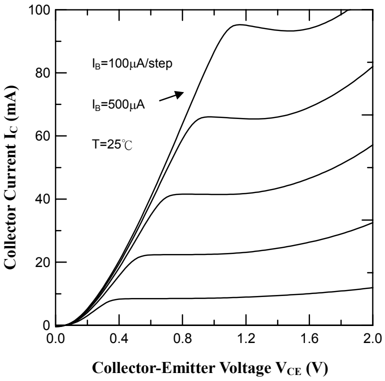

Fig. 1(c) Typical common-emitter I-V characteristics of the studied InP/InGaAs TEBT at high collector current regimes.

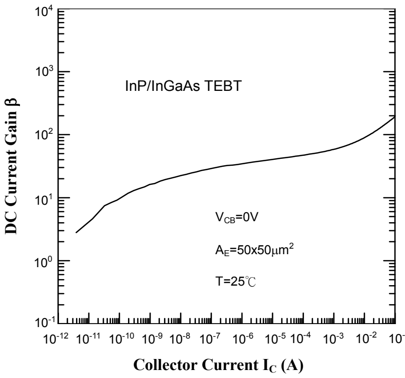

Fig. 2 Measured DC current gain as a function of collector current of the studied TEBT at V_{CB}=0V.

the lowest current level for transistor action. The current gain is increased to 191 at the collector current of I_C=9.95×10^{-2}A (3.98×10^{3}A/cm^2). The presence of current gain (>1) at ultra-low current region may be mainly attributed to negligible hole tunneling probability and the high quality base layer. These factors cause the considerable hole localization within the tunneling barrier and domination of base bulk recombination among the whole base current, respectively.

3. Conclusions

Due to the employment of an appropriate tunneling emitter barrier, holes are confined effectively. So, the emitter injection efficiency is remarkably enhanced. Experimentally, the studied TEBT device shows a very small offset voltage of 40mV and an extremely wide collector current operation regime. The operation region is larger than 11 decades in magnitude of collector current (10^{-12} to 10^{-1}A). A DC current gain β about 3 is obtained even the device is operated under an ultra-low collector current of 3.9×10^{-12}A (1.56×10^{-7}A/cm^2) without passivation structure. The common-emitter breakdown voltage of the studied device is higher than 2V. Consequentially, based on experimental results, the studied TEBT device offers the promise for low-power and low supply voltage electronics applications.

Acknowledgements

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