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Improvement of DC and RF characteristics of AlGaN/GaN HEMTs by thermally annealed Ni/Pt/Au Schottky gate

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1. Introduction

AlGaN/GaN high electron mobility transistor (HEMT) is a candidate for high power and high frequency applications. Recently, high performances have been demonstrated [1,2]. However, there remain a lot of issues to be investigated. One of them is the fabrication of a high quality Schottky gate, which is required to ensure the enough gate-control characteristics [3]. Until now, we have investigated a thermal annealing effect on Ni(Ti)/*x*/Au Schottoky electrodes, where *x* stands for the various metals [4]. The combination of the thermal annealing with a high work function metal insertion was found to improve the Schottky characteristics such as barrier height (Φ).

In this paper, we fabricated AlGaN/GaN HEMTs whose Schottky gate consisted of Ni/Pt/Au had been subjected to a rapid thermal annealing (RTA). This gate RTA technique successfully improved both DC and RF characteristics of HEMTs.

2.Experimental

Figures 1 and 2 show fabrication process and schematic structure of HEMTs. At first, AlGaN/GaN HEMT epilayers were grown by metal organic chemical vapor deposition. After forming the source/drain ohmic contacts of Ti/Al/Ti/Mo/Au and the implant isolation of Zn ions, we started to fabricate the Schottky gates. The Ni/Pt/Au gate electrodes were patterned by the e-beam evaporation and lift-off technique. The thicknesses of Ni, Pt and Au were 3, 30 and 300 nm, respectively. Then, the gate RTA of 600 ºC for 5 minutes in nitrogen ambient was performed. Lastly, silicon nitride film (SiN) with thickness of 100 nm was deposited by plasma enhanced CVD. The gate length (L_g) and the unit gate width (W_{gu}) were 1 and 75 μm, respectively. RF measurements were carried out on wafer.

3. Results and discussion

Figure 3 shows current-voltage (*I-V*) characteristics for Schottky diodes fabricated in the same wafer as the HEMTs. Ideality factor (n factor) and Φ were extracted by using a thermionic emission model. The Schottky characteristics were obviously improved by utilizing the gate RTA, that is, the Φ increased from 0.61 to 0.82 eV, and the n factor decreased from 4.0 to 2.1. We expected that there were two effects in the gate RTA. One was that Pt was diffused to the AlGaN surface and formed the metal-semiconductor interface with the higher barrier height. Another was that Ni reacted with the AlGaN surface, which reduced an interface trap causing an anomalous leakage current.

Figure 4 shows the effects of the gate RTA on the transistor characteristics, which were measured before and after the gate RTA. From the gate voltage (V_g) dependence of the drain current (I_d) (Fig. 4(a)), the threshold voltage (V_{th}) shifted toward higher V_g due to the increase of the Φ. On the other hand, maximum transconductance (g_{mmax}) was not affected by the gate RTA and exhibited around 140 mS/mm, as shown in Fig. 4(b). Moreover, it was revealed that the off-state breakdown voltage (BV_{off}) rose from 107 to 178 V in Fig. 4(c). This is attributed to the reduction of the gate leakage current owing to the improvement in Schottky characteristics. It should be commented that the ohmic contacts and the device isolation were not degraded through the gate RTA.

Device passivation with SiN is usually used in order to reduce a current collapse. We confirmed that I_d measured with pulsed V_g improved by SiN deposition as summarized in Fig. 5.

It is well known that SiN passivated devices suffer from the degradation of the breakdown voltage [2]. In our experimental, the SiN passivated devices without the gate RTA had the poor BV_{off} of less than 80 V. However, the remarkable feature of high BV_{off} of 120 V was successfully recorded in the HEMTs with the gate RTA as shown in Fig. 6(a). The gate RTA technique maintained the high BV_{off}, because of the increased BV_{off} in advance (Fig. 4(c)). Figure 6(b) shows I_d-V_d curves. The high V_g of +3 V can be applied, and I_d of as high as 1 A/mm was obtained regardless of the long L_g of 1 μm. Figure 6(c) shows the transfer characteristics. Although the V_{th} was changed by the deposition of SiN, g_{mmax} was preserved.

Figure 7 shows cutoff frequencies (f_t) and maximum frequency of oscillation (f_{max}) as a function of V_g. For comparison, we also fabricated both unpassivated and passivated samples without the gate RTA. High f_t was obtained for the passivated HEMTs with the gate RTA in the wide V_g range in Fig. 7(a). In addition, the comparable f_{max} to that of the unpassivated HEMT was obtained in the HEMTs with the gate RTA in spite of the increased parasitic capacitance by SiN, as shown in Fig. 7(b). These improvements suggest that the gate RTA progress the qualities of the interface between the Schottky gate and the AlGaN.

4. Conclusions

The thermal annealing effects on AlGaN/GaN HEMT with Ni/Pt/Au gate were investigated. The n factor and Φ of the gate Schottky diode were drastically improved by the thermal annealing. In HEMTs characteristics, BV_{off} increased by the gate RTA, and BV_{off} as high as 120 V was obtained even after SiN deposition. V_{th} changed due to the increase of Φ. In the RF measurement, high f_t and f_{max} were obtained as compared with SiN passivated HEMT without the gate RTA.

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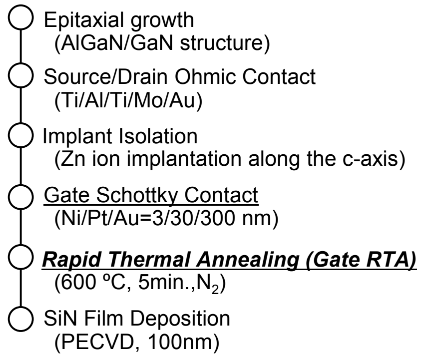


Fig. 1 Fabrication process of HEMT.

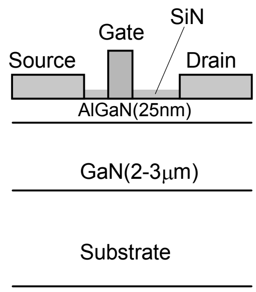


Fig. 2 Schematic structure of HEMT.

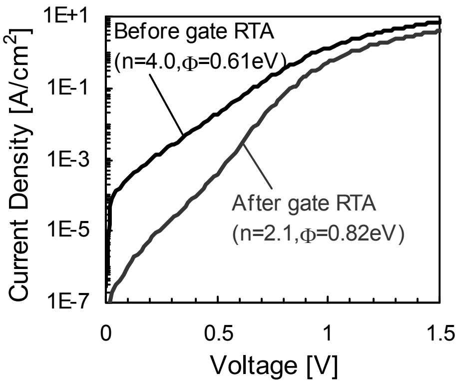
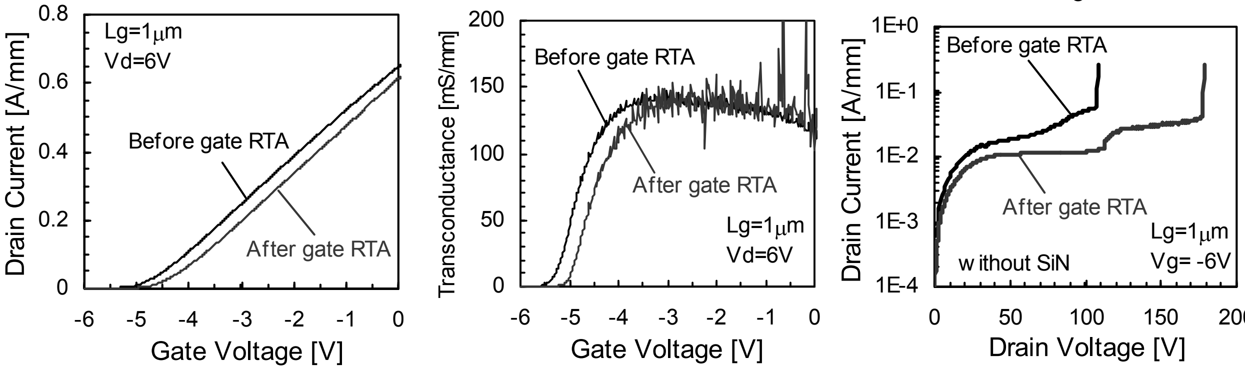


Fig. 3 Current-voltage curves of Schottky diodes before and after gate RTA.



(a) (b) (c)

Fig. 4 Transistor characteristics before and after gate RTA. (a)Drain current-gate voltage curves. (b) Transconductance-gate voltage curves. (c)Drain current-drain voltage curves below pinchoff voltage.

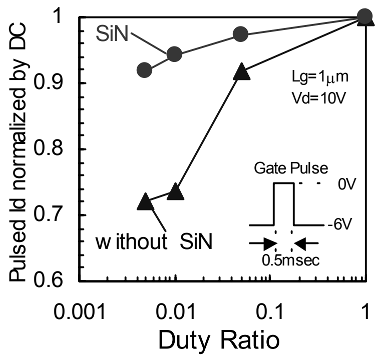
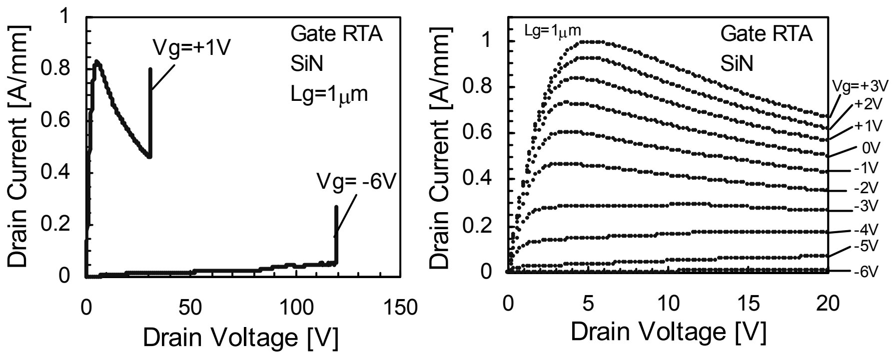


Fig. 5 Pulsed drain current normalized by DC value as a function of the duty ratio.



(a) (b)

Fig. 6 Characteristics of SiN passivated HEMT with gate RTA. (a) On-state and off-state breakdown. (b) Drain current-drain voltage curves.

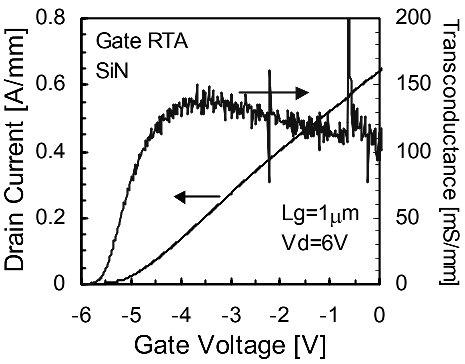
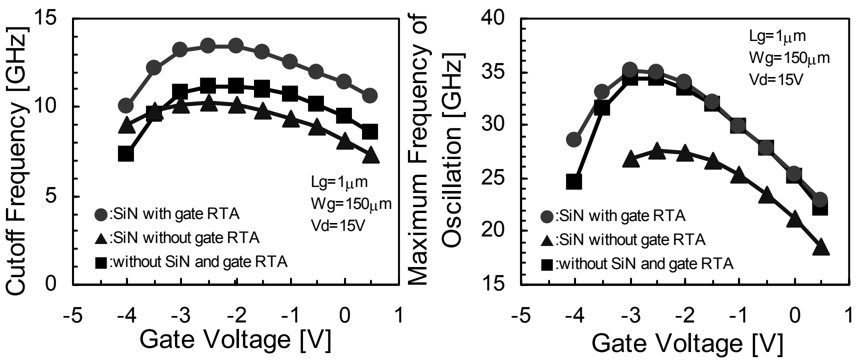


Fig. 6 (c) Transfer characteristics of SiN passivated HEMT with gate RTA.



(a) (b)

Fig. 7 (a)Cutoff frequency and (b)maximum frequency of oscillation as a function of the gate voltage.