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ESD Circuit Simulation Technology Using Protection Device Model with Generated-Hole-Dependent Base Resistance

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1. Introduction

In the development of VLSI technologies, ESD (ElectroStatic Discharge) is one of important issues in the reliability. MOS-based protection circuits are commonly used in current technologies and the high current behavior of MOS transistors determines the ESD robustness of VLSI circuits. Circuit simulations are important to examine the design of ESD protections and an accurate protection device model is indispensable [1-3]. Suzuki et al. pointed out that generated holes, as well as injected electrons, modulate the base resistance during the snapback [3]. In this paper, we propose an equivalent circuit model for MOS protection devices, which includes the generated-hole-dependent base resistance. Circuit simulations using our equivalent circuit model well reproduced measured snapback characteristics and results show the effectiveness of our model.

2. Equivalent circuit model

Our equivalent circuit model for the MOS protection device is shown in Fig. 1. The parasitic elements, a bipolar transistor , two current source (I_{LeakC} and ξI_C), and the modulated base resistance, are combined with the MOS transistor model (we use BSIM3). The parasitic bipolar transistor plays a dominant role in snapback characteristics. I_{LeakC} is a leak current due to electron-hole pairs occurred thermally in the junction depletion layer. The hole current ξI_C (ξ ; impact ionization rate) is due to the impact ionization. In addition, the modurated base resistance is expressed as R_{BS} and R_{B0}, which are connected in parallel.

We assumed a MOS structure without the gate (Fig. 2) so that we could focus on the parasitic elements. We use the HSPICE for circuit simulations and use the Medici for device simulations. We extracted I_{LeakC} from the Medici data and modeled them by setting up a table. Parameters of a bipolar transistor, a coefficient ξ , the base resistance R_{BS} (modulated by injected electrons) and the constant R_{B0}, and source and drain resistances R_S and R_D, are also extracted from the Medici data .

Fig. 3 shows the Gummel plots of the parasitic bipolar transistor. HSPICE results well reproduce Medici results. But we must modified the resistance R_{BS}. When the hole current flows from the substrate dominantly ($I_B > \xi I_C$), the base resistance varies. When the hole current flows from the drain dominantly ($I_B < \xi I_C$), R_{BS} is modulated by generated holes and the base resistance is the constant (Fig. 4). If we ignore this modulation by generated holes, the snapback characteristic does not reproduce the Medici result (Fig. 5).

Our equivalent circuit model (Fig. 1) represents the gate bias dependence of snapback characteristics. Fig. 6 shows snapback characteristics of HSPICE compared with those of Medici. HSPICE results almost reproduce the gate voltage dependence of snapback characteristics in Medici results.

We modified the equivalent circuit parameters (Rs, Rd, R_{Well} ,and ξ) to reproduce measured snapback characteristic (Fig.7 (a) and (b)). Measured results were obtained using TLP (Transmission Line Pulsing) measurement [4] for an nMOS or a pMOS test structure. The HSPICE result with modified parameters well reproduced the measurement result.

3. ESD circuit simulation

We applied our model and extracted parameters to ESD circuit simulations. Fig. 8 shows the test protection circuit with multi-finger MOS devices. We compared circuit simulation results with TLP measured results (Fig. 9 (a) and (b)). When V_{DD} is floating, ESD stress flows from the pad to nMOS devices. On the other hand, when V_{SS} is floating, ESD stress flows from the pad to pMOS devices. Simulated results well agreed with measured results. These results suggest that if we properly extract parameters from a MOS device, we can carry out accurate simulation for the circuits.

Fig. 10 shows another simulation example for a typical I/O circuit. We applied our model to ESD protection and driver transistors, and carry out HSPICE simulation under HBM (Human Body Model) condition. The snapback characteristic for the circuit is shown. Our simulation technologies are applicable for arbitrary I/O circuits that include MOS protection devices to examine the protection design.

4. Conclusions

We proposed an equivalent circuit model for MOS protection devices, which included a parasitic bipolar transistor with generated-hole-dependent base resistance, and applied it for ESD circuit simulations. Simulation results for the protection circuit with multi-finger MOS devices well reproduced measured snapback characteristics. These show the effectiveness of our ESD circuit simulation technology.

References

[1] A. Amerasekera et al, *Proc. IEEE 1996 International Reliability Physics Symposium,* (1996) *p. 318.*
[2] M. Mergens et al., *Proc. 2000 EOS/ESD Symposium,* (2000) *p.446.*
[3] K. Suzuk et al., *Proc. IEEE 2001 International Reliability Physics Symposium,* (2001) *p.246.*
[4] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits, John Wiley & Sons, New York, Inc., 2002.*

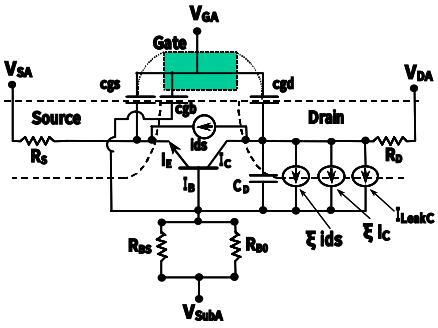


Fig. 1. An equivalent circuit model.

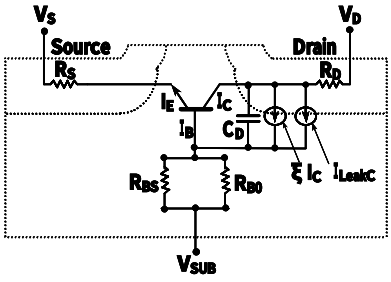


Fig. 2. Parasitic elements in the protection device.

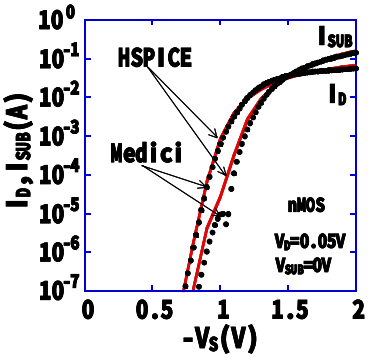


Fig. 3. Gummel plots of parasitic bipolar transistor.

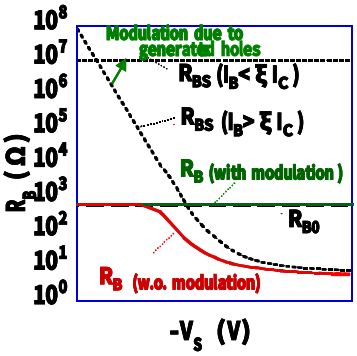


Fig. 4. Base resistance.

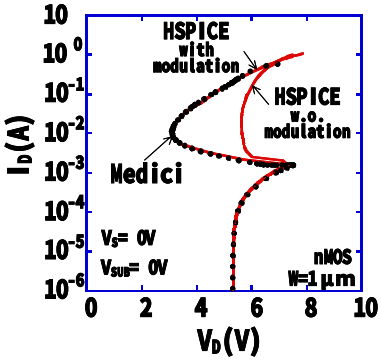


Fig. 5. Snapback characteristics in the parasitic device.

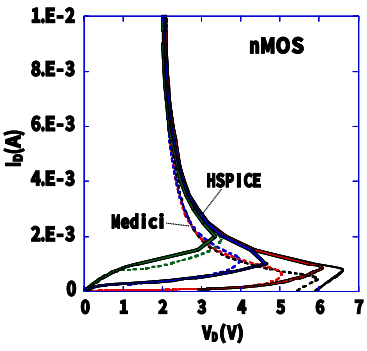
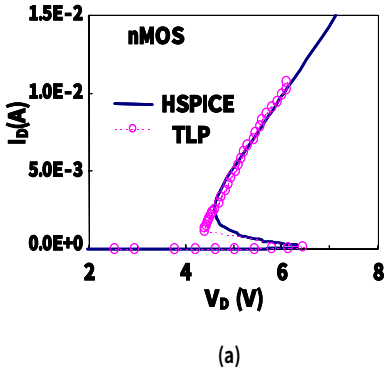


Fig. 6. Snapback characteristics in the protection device. Vg=0, 0.5, 1.0, and 2.0 V.



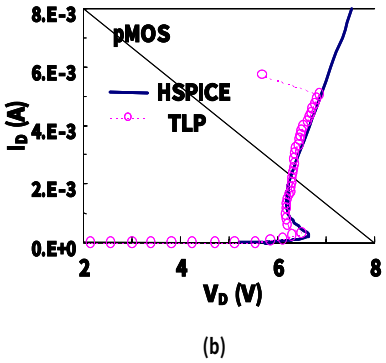


Fig. 7. Snapback characteristics in the MOS transistors. (a) nMOS and (b) pMOS.

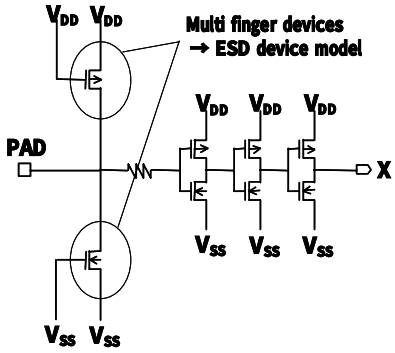
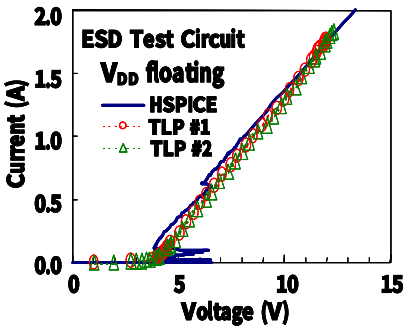


Fig. 8. An ESD protection circuit.



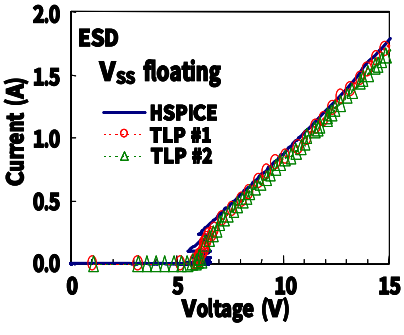


Fig. 9. Snapback characteristics in the protection circuit. (a) V_{DD} floating and (b) V_{SS} floating.

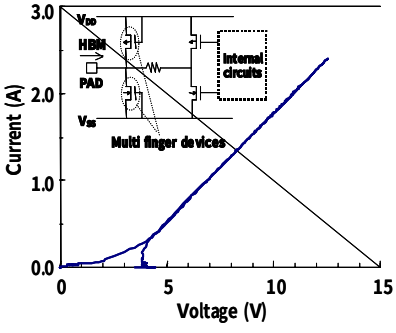


Fig. 10. Snapback characteristics under the HBM stress in a typical I/O.