Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 376-377

G-4-1 (Invited)

3D System Integration by Chip-to-Wafer Stacking Technologies

Peter Ramm, Armin Klumpp, Reinhard Merkel, Josef Weber, Robert Wieland, Günter Elst[1]

Fraunhofer Institute for Reliability and Microintegration, Munich Division
Hansastrasse 27d, 80686 Munich, Germany
Phone: +49-89-54759-539 E-mail: peter.ramm@izm-m.fraunhofer.de
[1]Fraunhofer Institute for Integrated Circuits, Dresden Division
Zeunerstrasse 38, 01069 Dresden, Germany

1. Introduction

Worldwide several outstanding technologies for 3D system integration are currently in development, a few of them are already in production. Successful market entry is determined by the performance improvement achieved and the profitability in relation to the total system cost. Manufacturing technologies based on wafer fabrication processes show the potential of a comparatively favorable cost structure. On the other hand wafer yield and chip area issues may speak against wafer stacking concepts. In consequence, chip-to-wafer technologies largely relying on wafer-level processes utilizing known good dice only, will be of advantage. A corresponding new approach for vertical system integration is introduced and discussed. This so-called ICV-SLID technology is based on adjusted bonding and vertical metallization of completely processed device substrates without interfering the basic IC process.

2. Vertical System Integration

Vertical system integration based on direct InterChip Vias (ICV) with lateral dimensions of a few microns, leads to a very high integration density of the inter-chip wiring of stacked devices. Modeling of the signal interconnection structure of vertical integrated ICs shows that the ICVs will not degrade signal transmission [5]. So the integration of complex high performance systems can be realized on a single stack of chips. Corresponding concepts in principle are suitable for both, wafer stacking and chip-to-wafer stacking. Thinned device substrates (wafers or dice, respectively) are stacked by aligned bonding and electrically interconnected by free positioned inter-chip vias. Fraunhofer IZM in cooperation with Infineon Technologies developed a wafer-to-wafer stacking technology based on low temperature bonding with polyimide as intermediate layer and a vertical wiring using W- or Cu-filled inter-chip vias. Wafer stacks fabricated according to the so-called InterChip Via technology showed a very high vertical interconnect density of some 10^5 cm^{-2} with low contact resistance inter-chip vias in the range of 1 - 3 Ohm. Although the reported results are promising [1, 2] wafer yield and chip area issues in general may speak against wafer stacking concepts: Yield loss by stacking of a non functional die to a good die, and even more serious, different step sizes and chip sizes (with loss of active silicon area), result in an increase of the total cost per 3D-stack. A chip-to-wafer stacking approach was reported by Infineon Technologies and Fraunhofer IZM [3]. Both, the mechanical and the electrical connections between the chips are realized by solid-liquid-interdiffusion [4] of thin electroplated Cu/Sn layers. This face-to-face technology has the potential for low cost fabrication but on the other hand – as non-modular concept – is limited to applications with two layer stacks.

In consequence we are working on the development of a new chip-to-wafer stacking technology which combines the advantages of the ICV process and the solid-liquid-interdiffusion technique (SLID). The fully modular ICV-SLID concept allows the formation of multiple device stacks. The schematic cross section of a corresponding 3D integrated circuit is shown in Fig. 1. Aligned stacking of a 3rd level chip is also indicated in the figure. The starting materials for the chip-to-wafer approach ICV-SLID are completely processed and tested device wafers. For a first evaluation a test chip with 3D integrated structures was designed in order to characterize the inter-chip interconnections. 200 mm wafers with metallization layers and inter-level dielectrics were processed according to the ICV-SLID process flow. First step of the 3D integration sequence is the formation of inter-chip vias by deep trench etching, lateral isolation and metal filling. Typically 1 - 3 µm diameter vias are prepared on the top wafer. These high aspect ratio ICVs are etched through all dielectric layers and typically 12 µm deep into the silicon. The via trench is laterally isolated with highly conformal O_3 /TEOS and finally refilled with TiN/W CVD. Subsequently, a tungsten etch back process is applied for W-plug formation. The lateral electrical connection of the metallized inter-chip via with the metal level of the top wafer is done by opening contact windows on the top wafer followed by a standard Al metallization and passivation. The wafer is then temporarily bonded onto a handling substrate by using a glue polymer and thinned with high uniformity until the ICVs are opened from the rear (remaining silicon thickness approximately 10 µm). After deposition of dielectric layers for electrical isolation and opening to the W-filled inter-chip vias, through-mask electroplating of a

typically 8 µm thin copper/tin bilayer is applied. The bottom wafer is through-mask electroplated with Cu as the counterpart metal of the soldering metal system. A 3D integrated test structure after SLID and removal of the handling substrate is shown in Fig. 2.

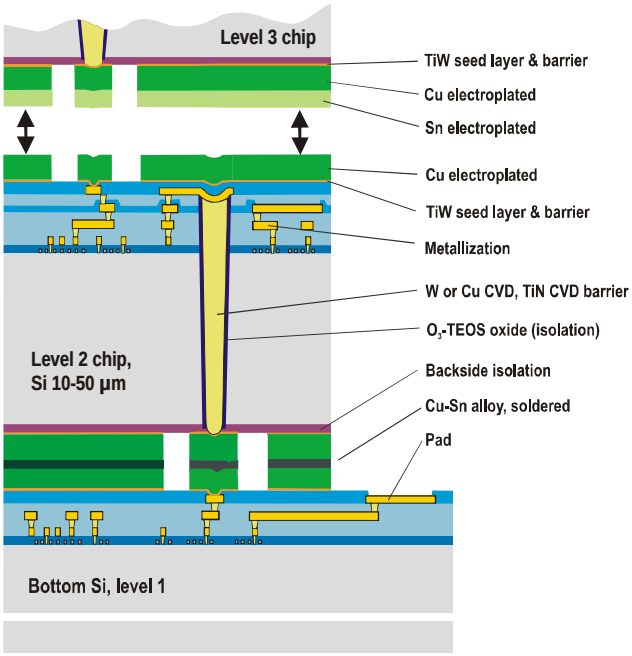

Fig. 1: Schematic cross section of a corresponding 3D integrated circuit with the fully modular ICV-SLID concept

The device stack is now ready for addition of the 3rd level chip (principle shown in Fig. 1). The process

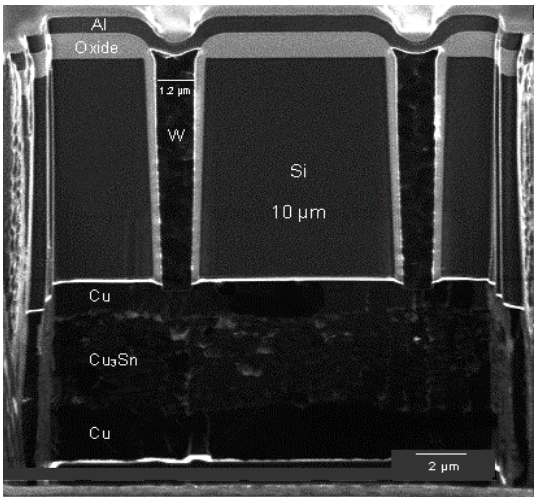

Fig. 2: Cross section (FIB) of 2-level stack with ICV-pins, 10 µm silicon and SLID metal system.

sequence is identical to the one used for the 2-layer-stack, for the process concept is completely modular. Fig. 3 shows the cross section (FIB) of a three-layer stack. The 10 µm thin medium chip is connected to the bottom device wafer by the SLID system (Cu, Cu_3Sn e-phase, Cu). The 3rd level chip is connected to the medium chip by the SLID technique as well.

Finally the bond pads are opened and the 3D integrated device stack can be tested, separated and mounted by use of standard procedures.

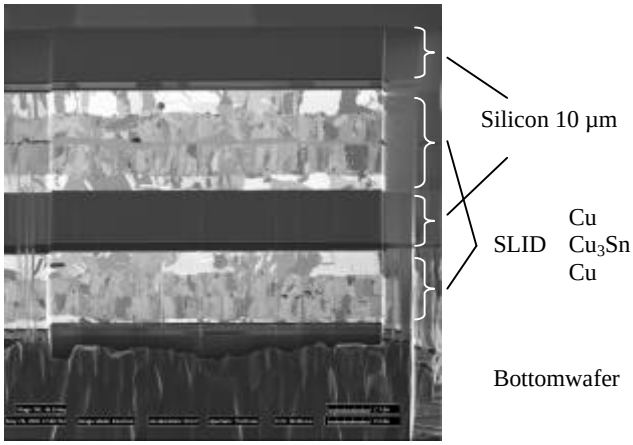

Fig. 3: Cross section (FIB) of a three-layer stack

3. Conclusions

A new approach for 3D system integration, is introduced. A test chip was designed and the total process sequence of the ICV-SLID technology for the realization of a three-layer chip-to-wafer stack was demonstrated. The proposed wafer-level 3D integration concept has the potential for low cost fabrication of multi-layer high-performance 3D-SoCs and is well suited as a replacement for embedded technologies based on monolithic integration.

Acknowledgements

This report is partly based on a project which is supported by the German Bundesministerium für Bildung und Forschung under support-no. 01M 2999 A.

References

[1] P. Ramm, D. Bonfert, H. Gieser, J. Haufe, F. Iberl, A. Klumpp, A. Kux, R. Wieland, *Proc. International Interconnect Technology Conference (IITC 2001)*, (2001) p. 160

[2] P. Ramm, D. Bonfert, F. Iberl, A. Klumpp, S. Riedel, S.E. Schulz, R. Wieland, M. Zacher, T. Gessner, *Proc. Advanced Metallization Conference (AMC 2001), edited by A.J. Mckerrow, Y. Shacham-Diamond, S. Zaima, T.Ohba (Mater. Res. Soc. Proc. V-17, Warrendale)*, (2001), p. 159

[3] H. Huebner, O. Ehrmann, M. Eigner, W. Gruber, A. Klumpp, R. Merkel, P. Ramm, M. Roth, J. Weber, R. Wieland, *Proc. Advanced Metallization Conference (AMC 2002), edited by B.M. Melnick, T.S. Cale, S. Zaima, T. Ohba (Mater. Res. Soc. Proc. V-18, Warrendale)*, (2002) p. 53

[4] L. Bernstein, H. Bartolomew, *Trans. Met. Soc. AIME 236, (1966), p. 404*

[5] S.A. Kuehn, M.B. Kleiner, P. Ramm, W. Weber, *IEEE Trans. Comp., Packag., Manufact. Technol.-Part B, vol. 19, no. 4*, (1996) p. 71