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Micro Cu Bump Interconnection on 3D Chip Stacking Technology

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1. Introduction

Nowadays three-dimensional (3D) LSI stacking technology with through electrode is studied extensively [1]. This technology will realize high-density packaging and high operation performance. The 3D chip stacking is one of the technologies, which characterized to use conventional device-ready wafers, and the known-good-die (KGD) is confirmed before stacking [2]. Figure 1 shows a cross section of 3D chip stacking structure. The 10μm square Cu thorough electrodes (Cu TH via) are formed in the 20μm pitch through the Si devices at a 50 μm thickness, and exposed on the back surface of the each device. As for advanced flip chip bonding technology, Cu bump bonding (CBB) utilizing Sn-alloy as bonding material is low temperature bonding process expected to realize a simple interconnection of the Cu TH via. We have already investigated mechanism of Cu-Sn reaction and the connection of Cu bump through the Cu-Sn inter metallic compound (IMC) was confirmed [3]. It is considered that the IMC layer occupies a greater proportion of the whole joint. However, influence of the IMC on the minute interconnection reliability have not been enough studied yet because of poverty of mechanical data of IMC.

In this paper, the results of the experiments are introduced regarding with the analysis of determination of mechanical property of IMC and mechanical effect of IMC on 20μm pitch minute Cu bump interconnection.
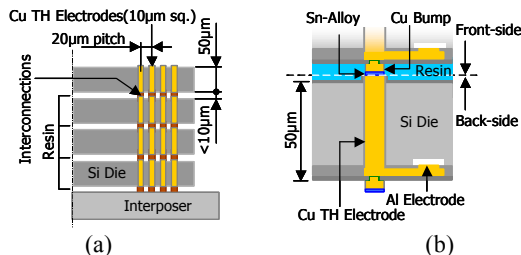

Fig. 1   Schematic diagram of (a) 3D LSI structure, (b) Cu TH electrode interconnections utilizing CBB.

2. Experiment

First, a young's modulus of Cu-Sn IMC thought to be most relevant mechanical property was measured by the nano-indentation, which can evaluate the thin layer with the control of the minute indenter in nanometer scale. Figure 2 shows the experimental model and procedure. The electroplated Cu bumps with electroplated Sn2.5Ag-coat were formed on the Si chip, and annealed (300°C/1min or 400°C/5min) in an inert gas to make IMC layer on the surface. The bump surface was measured by nano-indentation, and the chemical composition of the indentation point was analyzed by energy dispersive X-ray (EDX) analysis. Next, in order to estimate the mechanical effect of the interface material on the

interconnection reliability, we conducted finite element method (FEM) on two-dimensional elastic-plastic thermal analyses for temperature cycling (125°C / -40°C). Figure 3 shows the analysis model. Finally, 3D chip stacked module was built according to the results of FEM analysis.
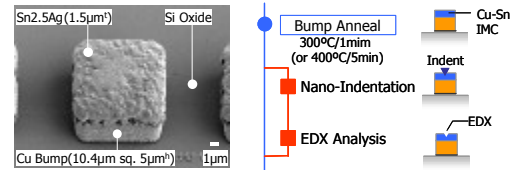

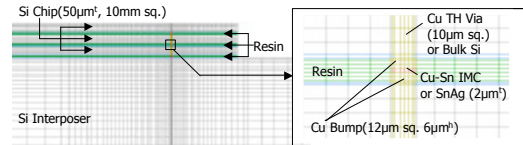Fig. 2   Experimental model and procedure for evaluation

Fig. 3   Ultra-thin Die stacking model for FEM analysis.

3. Results and Discussion

Mechanical properties of Cu-Sn IMC

Figure4 shows Load-displacement curves measured at maximum load of 300μN for the bump surface material after anneal. The elastic recovery was confirmed during unloading of indenter. The curves were stable and dependence of anneal condition was identified. Thus, elastic deformation behaviors of surface material were successfully measured without influence of Cu base. Table 1 shows the result of experiments. The young's modulus for Cu_6Sn_5 (112.58GPa) and Cu_3Sn (132.66GPa) were obtained. The values of this research were comparable to previously published values [4]. And, it was considered that bonding interface was formed by isothermal solidification of liquid phase into Cu_6Sn_5 at the low bonding temperature above melting point of Sn-alloy. Therefore, 110GPa was applied to FEM analysis as approximation of young's modulus of Cu_6Sn_5.
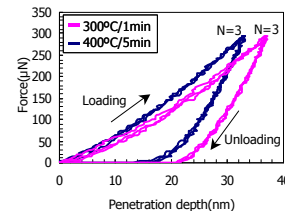

Fig. 4   Load-displacement curves of the bump surface material.

Table 1   Mechanical properties of IMC by nano-indentation.

Anneal Conditions	EDX result	Young's Modulus (GPa)	
		Present Data	Fields et al.[4]
300°C /1 min	Cu_6Sn_5	112.58	85.56
400°C /5 min	Cu_3Sn	132.66	108.3

Mechanical effect of interface material on interconnection

FEM analysis was performed utilizing the material properties listed in Table 2. Figure 5 shows the result of focused on equivalent plastic strain range (Δe_{eq}) of Cu bump. As the results, Δe_{eq} depends on CTE of resin at each condition. And this dependence is reduced in the cases where the bonding interface is composed of IMC. It is considered that a stress caused by thermal mismatch in the thickness direction between the minute interconnection and the resin cannot be neglected even as Si on Si structure. Although the stress caused plastic deformation of SnAg layer easily, rigid Cu and IMC layer are hardly deformed. In addition, Δe_{eq} of Cu bump with SnAg layer is decreased in case with Cu TH via. As the thermal deformation of Cu TH via is much larger than that of Si chip, the Cu via restrains the deformation of SnAg layer. Meanwhile, the deformation of Cu TH via acts to pull Cu bump with IMC layer, and Δe_{eq} is increased. Despite increase of Δe_{eq}, Cu bump with IMC layer is smaller totally. Therefore, it is acceptable that the SnAg layer as bonding material is well diffused and reduced to Cu-Sn IMC.

Table 2   Material properties for FEM analysis.

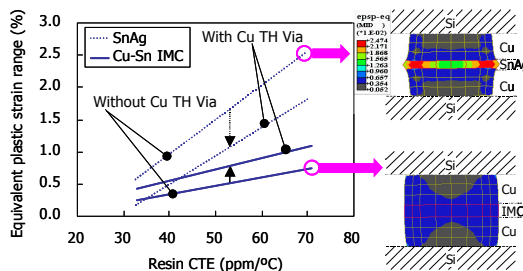| Material	Filler Contents (wt%)	Young's Modulus (GPa)	Poisson's Ratio	CTE (ppm)	Yield Stress (MPa)
Cu	---	110	0.3	17	100
SnAg	---	40	0.3	23	40
Cu-Sn IMC	---	110	0.3	23	150
Si	---	190	0.07	3	---
Resin	0-60	3.2–8.5	0.3	71-33	---

Fig. 5   Equivalent plastic strain range of Cu bump.

Figure 6 shows the result focused on principal stress distribution of resin (60wt% filler) around interconnection without Cu TH via. The stress around Cu bump is higher than Au bump, which confirmed sufficient interconnection reliability [5]. As previously noted, Cu bump with IMC are hardly deformed, and don't absorb the thermal stress. In addition, rigid resin with high filler content has less effect on reduction of own thermal stress. Therefore, low filler content resin is preferable for Cu bump interconnection differently from Au bump interconnection. Additionally, the low viscosity resin due to low filler content can easily encapsulate the ultra-thin gap between devices.
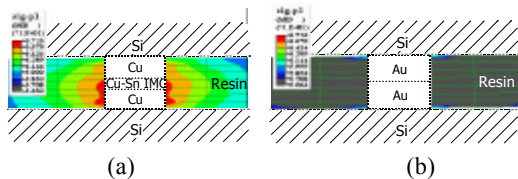

Fig. 6   Principal stress distribution of resin (60wt% filler) around (a) Cu bump include IMC, (b) Au bump without Cu TH via.

Interconnection of Cu bump through Cu-Sn IMC layer

Next, the vertical interconnections in 20µm pitch between the Cu TH via with Cu bump coated Sn2.5Ag and the Cu bump was performed. Figure 7 shows the experimental model and Procedure. The chip was stacked after dispensing low rigid non-conductive particle paste (NCP) onto the interposer [6]. The bonding temperature was set at 240°C above Sn2.5Ag melting point, and the gap was fully encapsulated by NCP.
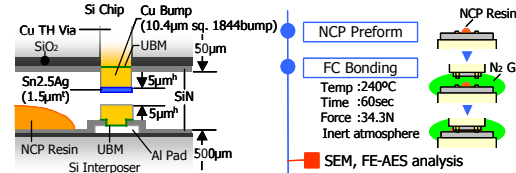

Fig. 7   Experimental model and procedure.

Figure 8 (a) shows SEM image of entire cross section of micro joint. No remarkable damage around under bump structure was found. Figure 8 (b) shows the result of auger electron spectroscopy (AES) mapping for the profile of Sn, Cu and Ag on the bonding area. As shown in the result, the initial Sn2.5Ag was completely reduced to Cu-Sn IMC. Therefore, optimal interconnection based on FEM analysis was achieved.
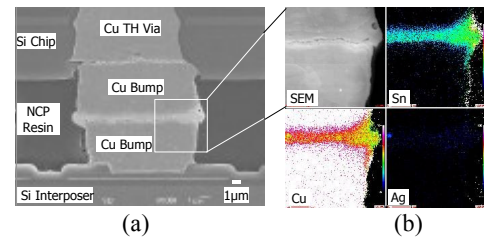

Fig. 8   Analysis of interconnection indicate (a) SEM image of entire cross section, (b) FE-AES mapping.

4. Conclusion

1) Young's modulus of Cu-Sn IMC (Cu_6Sn_5:112.58GPa and Cu_3Sn:132.66GPa) were obtained by nano-indentation.

2) SnAg layer as bonding material should be reduced to Cu-Sn IMC, and low rigid resin was preferable by FEM analysis.

3) The vertical interconnections utilizing Cu bump in 20µm pitch was performed with low rigid NCP encapsulation. The initial Sn2.5Ag was completely reduced to IMC, and optimal interconnection based on FEM analysis was achieved. Establishment of micro joint reliabilities will be the subject.

References

[1] M. Koyanagi, H. Kurino, K. Sakuma, K.W. Lee, N. Miyakawa and H. Itani: IEEE Micro, **18** (1998) No. 4, 17.

[2] K. Takahashi, H. Terao, Y. Tomita, Y. Yamaji, M. Hoshino, T. Sato, T. Morifuji, M. Sunohara and M. Bonkohara: Jpn. J. Appl. Phys. **40** (2001) 4B, 3032.

[3] Y. Tomita, M. Tago, Y. Nemoto and K. Takahashi: *3rd Int. Symp. Electron. Mater. Packaging*, Jeju, 2001, p.107.

[4] R. J. Fields and S. R. Low: Research Publication of NIST.

[5] M. Umemoto, Y. Tomita, T. Morifuji, T. Ando, T. Sato and K. Takahashi: *52nd Electron. Comp. Technol. Conf.*, San Diego, 2002, p.1454.

[6] M. Umemoto, K. Tanida, Y. Tomita, T. Ando and K. Takahashi: *4th Electron. Packaging Technol. Conf.*, Singapore, 2002, p.285.