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Fabrication of High-Density Wiring Interposer for 10 GHz 3D Packaging Using a Photosensitive Multiblock Copolymerized Polyimide

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1. Introduction

By advancement in the operational speed and integration density of LSI chips, high performance computing systems have been realized until now. The clock frequency in a CPU-LSI chip is exceeding the GHz range. However, in order to realize a computing system with a higher performance, it is required performance up of not only components of computing systems but also LSI packagings and interconnects.

Polyimide is one of the most stable organic polymers because it has a glass transition temperature higher than 400 °C. Good electric properties of a high breakdown voltage of more than 1 MV/cm and a low dielectric constant of about 3.0 were already performed. Therefore, polyimide is used in an extensive applications, particularly electronic packaging and LSI passivation layers. However, conventional photosensitive polyimide has the drawback that it must be handled carefully at a temperature lower than 10 °C to avoid an exchange reaction, because the polyimide precursor of polyamic acid is highly unstable.

A new photosensitive polyimide is synthesized directly by block copolymerization using a catalyst in solvent at 180 °C. It is possible to synthesize various polyimides of many functional structures by copolymerization [1][2]. A photosensitive material is a diazonaphtoquinone (DNQ) compound. This polyimide has the attractive feature of high temperature thermal curing free, and thus offers the possibility of a low-temperature process. We have reported an interlayer dielectric process for semiconductor LSI circuits with another photosensitive polyimide synthesized using aromatic materials, to provide high thermal resistance [3]. Figure 1 shows the chemical structure of multiblock copolymerized polyimide. This polyimide structure is designed to have a low relative dielectric constant of 2.85 and a low tangent loss of 0.014 at 10 GHz (measured values).

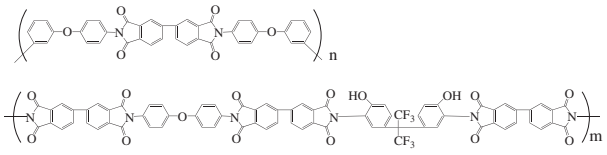

Fig. 1. Chemical structure of multiblock copolymerized polyimide.

We proposed a strip-line structure using the photosensitive polyimide with the aim of developing a high-density multilayer wiring package for IC packaging [4]. Impedance control can be performed in the strip-line structure to improve the high-speed signal transmission performance.

In this paper, we demonstrate high-density wiring interposer in which the photosensitive multiblock copolymerized polyimide is used as the insulator with the aim of developing a 10 GHz 3D packaging technology. By introducing a new polyimide, high-density wiring interposer with micron-sized transmission line was fabricated.

2. Fabrication

We fabricated the high-density wiring interposer using the multilayer structure of the photosensitive polyimide for the 10 GHz 3D packaging. The fabrication process of the interposer is described as follows. The process flow is shown in Fig. 2.

First, a gold groundplane 1 is formed on a silicon substrate using lift-off method (Fig. 2(a)). The photosensitive polyimide layer 1 is spin coated on the substrate, and is pre-baked at 100 °C for the photolithography process (Fig. 2(b)). Then the photosensitive polyimide layer 1 provides insulation between the groundplane 1 and the signal line layer. A g-line and h-line stepper is used to expose the lower via pattern (Fig. 2(c)). After exposure, the polyimide layer 1 is developed in an alkaline solution of N-methyl-2-phyrrolidone, 2-amino-ethanol and purified water (Fig. 2(d)) [5]. The polyimide layer 1 is post-baked at 290 °C. After post-baking, the polyimide layer 1 is treated by the Ar plasma irradiation (Fig. 2(e)). For the Ar plasma treatment, Ar gas pressure was 1.0 Pa, RF power was 1.2 W/cm^2, and discharge time was 1 min. A signal line photoresist pattern is formed on the polyimide layer 1. The signal line layer is fabricated by the deposition of gold metal film using a lift-off method (Fig. 2(f)). Next, the substrate is spin coated again by photosensitive polyimide to provide insulation between the signal line layer and

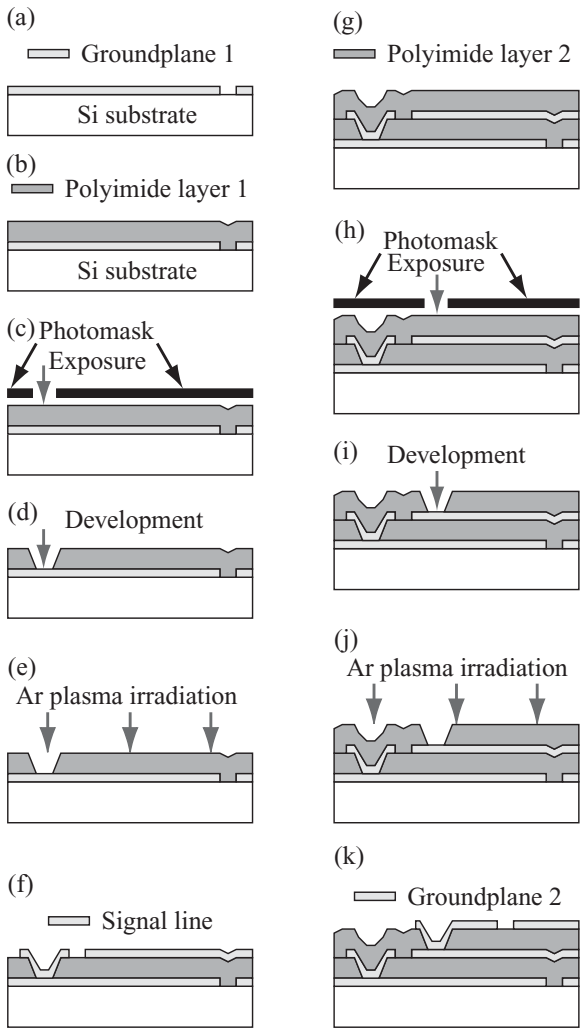

Fig. 2. Fabrication process.

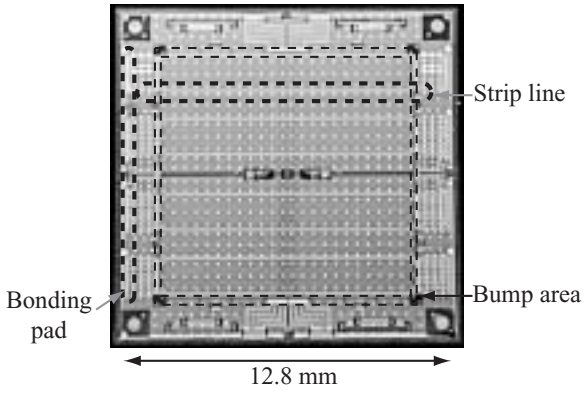

Fig. 3. Photograph of the high-density wiring interposer with micron-sized strip-line structures.

groundplane 2, and is pre-baked at 100 °C (Fig. 2(g)). A g-line and h-line stepper is used to expose the upper via pattern (Fig. 2(h)). After exposure, the polyimide layer 2 is developed and is post-baked at 290 °C and is treated by the Ar plasma irradiation (Fig. 2(i)(j)). Finally, the gold metal layer of groundplane 2 is deposited on the polyimide layer 2 using a lift-off method (Fig. 2(k)).

Figure 3 shows a photograph of the fabricated high density interposer. A size of this interposer is 12.8-mm square. Bonding pads and strip-line (Z_0 = 50 Ω) structures exist on the chip for GHz signal transmission testing. A width of main strip-lines is 12.5 μm. Widths of other strip-lines are 7.5 μm and 17.5 μm for test pattern. This interposer is capable of a 20-μm-pitched flip-chip connection at the bump area for 3D stacked LSI chips [6]. A size of the 3D stacked chips mounted on the interposer is 10.4-mm square. Thicknesses of gold signal line and gold groundplane 1 and 2 layers are 1 μm, respectively. 20 nm Titanium layer exists under gold layer for a barrier metal layer. In order to realize steady adhesion between the gold metal layer and polyimide layer, a thin Aluminum metal layer and a silane-coupling agent are coated on gold metal layer. The polyimide layer of about 8-μm thickness exists as insulation layer after development.

The micron-sized high-density wiring interposer was successfully fabricated using the photosensitive multiblock copolymerized polyimide as shown in Fig. 3.

3. Summary

By optimizing the method of multilayer photosensitive polyimide fabrication, we successfully demonstrated high-density wiring interposer in which the photosensitive multiblock copolymerized polyimide was used as the insulator with the aim of developing the 10 GHz 3D packaging technology. The electrical results of the fabricated interposer will be carry out by the time domain reflectometry (TDR) measurement and the vector impedance measurement.

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