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System Packaging and Embedded WLP Technologies for Mobile Products

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1. Introduction

Wafer Level Packaging is one of most important technology in the semiconductor industry today. Its primary advantages are its small form factor and low packaging cost. On the other hand, CASIO Computer CO., LTD. found out more important possibility in the original WLP technology.

Several silicon chip in the WLP structure are embedded in PWB and inter connected each other with copper direct wiring. This new system packaging technology has many advantages that can respond to the requirements for future mobile products.

2. General Instructions

The concept of system packaging

There are different field technologies in electric products. In the past, each technology has developed individually.
Semiconductor: larger scale integration, fine process
Packaging: fine pitch wire bonding, BGA, CSP
PWB: multi layer, fine pitch, micro via, build up
SMT: high accuracy, high speed, smaller components

However today, system designs of mobile products are increasingly implementing integrated system packaging strategies. (Fig. 1)

WLP Technology

The Wafer Level Packaging Technology is an example of an emerging packaging technology. (Fig. 2)

The CASIO's WLP architecture is shown in Fig. 3.
There are dielectric layer (PI), under bump metal (UBM), re-distribution layer (RDL), copper post (POST), encapsulation material and terminal solder.
In the case of this technology, both RDL and Post are thick electroplating copper. As the density and operating frequencies increase for the high-density module application, there are significant electrical and mechanical advantages to a WLP with a thick copper RDL and thick epoxy encapsulation applied.

Recently, as the popularity of WLP continues to grow, numerous high volume mobile application involving "design for WLP" have emerged.

EWLP Technology

From the point of view of entire system integration, technology for single chip package is not impotant any longer.
Mobile products are focused on small form factors and increased performance through higher performance processors and higher density memory devices. Currently, mobile phone applications are implementing system in package (SiP).
With increasing complexity, known good die (KGD) issue is becoming a serious problem.

CASIO COMPUTER CO., LTD. and CMK CORPORATION have developed a new SiP technology called the Embedded Wafer Level Package (EWLP).
The active components (semiconductor chip) in the WLP structure are embedded into the PWB during PWB manufacturing process.

Creating a SoC involves mixing different silicon technologies onto a single piece of silicon, while EWLP integrates the different technologies within a single piece of PWB module. The unique feature of this EWLP technology is that it doesn't contain any solder inter connection inside.
In addition to improved electrical performance, EWLP can enable the improvement of module reliability. (Fig. 4)
The EWLP sample shown in Fig. 5 including three chip in the WLP structure has almost same structure with SoC's.

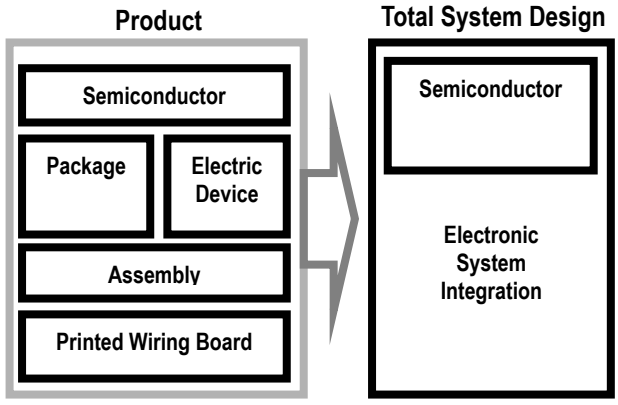

Fig. 1. System Packaging technology

Fig. 2. WLP Sample Wafer

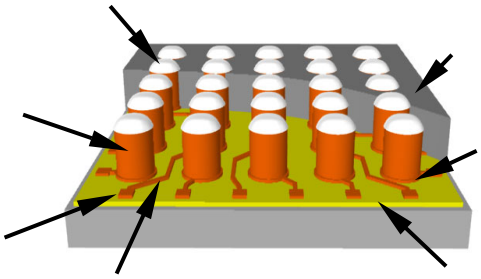

Fig. 3. Partial cross sectional view of CASIO's WLP

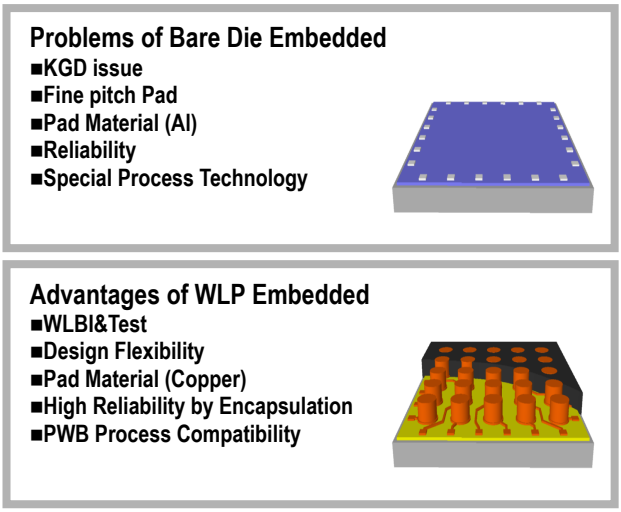

Fig. 4. Bare chip (die) vs. WLP

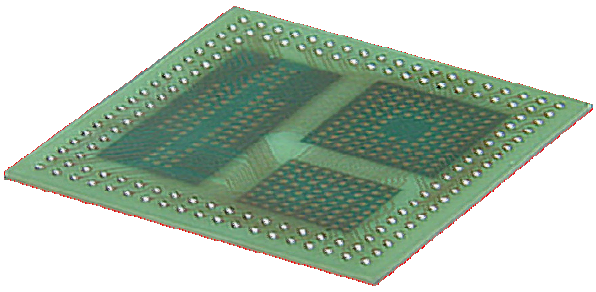

Fig. 5. EWLP Sample (Three WLPs are embedded)

3. Conclusions

In conclusion there are many challenges in the new embedded technology.

Fortunately, this time around we have the beginning of ideal WLP that go along way toward solving the KGD issue. At the same time, this WLP are embedded in PWB easily at lower cost.

Major semiconductor manufactures are moving toward supplying chip in this standard WLP formats.

Acknowledgements

Author would like to thank to entire EWLP development team at CMK CORPORATION for their dedication and efforts.

References

Appendix

DSP application in WLP format is shown in Fig. 6.

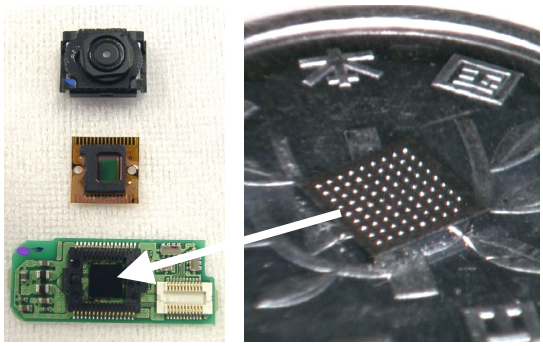

Fig. 6. DSP of camera module in cellular phone