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Evaluation of Hot-Carrier Hardness and Thick-Film Formation with STP Technique for Seamless Integration Technology

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1. Introduction

We have proposed seamless integration technology in which various kinds of large devices and structures 10- to 100-μm thick are stacked on CMOS LSIs to achieve new functionality [1]. This technology has been used to construct a MEMS fingerprint sensor comprising an array of 50-μm-square pixels as MEMS structures [2]. To seal the cavities of the sensor, we used the STP (Spin coating film Transfer and hot-Pressing) technique, in which a dielectric is transferred from a base film to the substrate by hot pressing [3, 4]. Although the sensor worked normally, the temperature and pressure during the hot-pressing step may degrade the underlying MOSFETs, especially considering that mechanical stress is known to degrade MOSFETs [5]. The influence of hot pressing on MOSFETs should therefore be clarified.

In addition, thick interconnects of 10 μm, called superconnects, have been proposed recently for the global interconnects of LSIs (Fig. 1) [6, 7]. However, it is difficult to fabricate them with simplicity.

In applying STP to form thick dielectrics on thick interconnects above MOSFETs as shown in Fig. 1, two fundamental issues should be clarified; formation characteristics of thick dielectrics and influence of hot pressing on MOSFETs for long-term reliability. In the present study, we examined gap-filling and planarization of 20-μm-thick dielectrics on 10-μm-thick interconnects and investigated the characteristics of MOSFETs after STP by hot-carrier injection.

2. Experiments

We used photosensitive low-k polyimide as 20-μm-thick dielectrics and Si substrate with 10-μm-thick Au interconnects. To assess the hot-carrier hardness of MOSFETs, we performed film-formation in severer conditions than that in Fig. 1: Dielectrics about 1.5-μm thick were formed directly on the MOSFETs by STP. The pressure and temperature in the hot-pressing step were 0.8 to 17.5 kPa and 80 to 120 ° C, respectively (Table I). We used lightly doped drain-structured n channel (n-ch) MOSFETs whose poly-Si gates were 0.5-μm long and 20-μm wide. The gate oxide was 11-nm thick.

Hot carrier stresses were imposed at bias conditions giving the maximum substrate current at drain voltage V_D ranging from 4.5 V to 5.3 V. After stressing, device degradation was evaluated from the threshold voltage shift ΔV_{th} and reduction rate of the maximum transconductance $\Delta g_m/g_m$ at $V_D = 0.1$ V.

3. Thick-Film Formation

The results of thick-film formation are shown in Fig. 2. The 20-μm-thick film filled the gap between interconnects and planarized the surface. Figure 3 shows the planarization characteristics versus pattern-density. We defined angle θ, planarization ability f, and pattern density d as shown in Fig. 3. Planarization ability corresponds to the degree to which the unevenness over the interconnects was planarized. Experimental results show that θ's were over 88 ° and the values of f were nearly 0 for a wide range of d. These results clarify that STP can planarize a surface for various pattern densities of thick interconnects.

4. Hot-Carrier Hardness of MOSFET

To evaluate device reliability before and after STP, hot-carrier stress tests were performed for n-ch MOSFETs in Fig. 4. The I_D-V_G characteristics in Fig. 5 before and after STP show no leakage current and the same tendency. The effects of hot-carrier injection on ΔV_{th} and $\Delta g_m/g_m$ are shown in Fig. 6 as a function of pressure in the hot-pressing step. There is no difference from the control sample and no dependence on the pressure. The dependence of hot-carrier lifetime on substrate current, I_{sub}, per unit channel width is shown in Fig. 7 with temperature in the hot-pressing step as a parameter. The lifetime was defined as the time when $\Delta g_m/g_m$ reached 10 %. The lifetime for the 120 °C process was on the same order as that for the 80 °C process, and they did not differ from the control sample. The lifetime at I_{sub}/W_g of 0.135 μA/μm (corresponding to V_D of 3.3V) was estimated to be over ten years for the sample in the 120 °C process. These results assure that STP does not damage MOSFETs for long-term reliability.

5. Summary

We showed that the STP technique is applicable to 20-μm-thick film formation and the surface was planarized for various pattern densities. The hot-carrier stress tests clarified that STP does not damage the MOSFETs at all. These results indicate that STP allows us to integrate thick structures and films on CMOS LSIs to achieve devices having new functionality for seamless integration technology.

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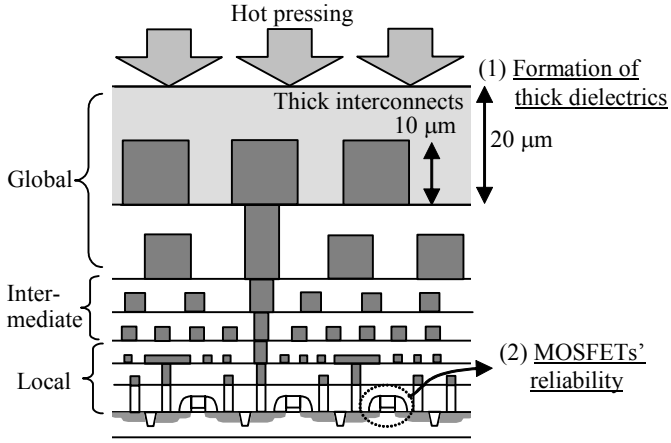

Fig. 1. Cross-section of multilevel interconnects architecture.

Table. I STP process conditions for each sample wafer.

Sample No.	STP process conditions
1 (Control)	Spin-coating
2	T = 120 ºC, P = 17.5 kPa
3	T = 120 ºC, P = 6.5 kPa
4	T = 120 ºC, P = 0.8 kPa
5	T = 80 ºC, P = 17.5 kPa

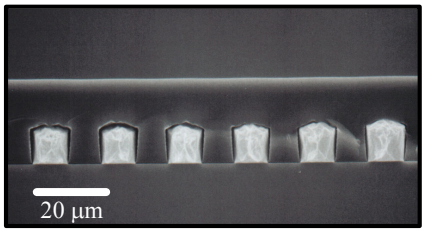

Fig. 2. SEM micrograph of a 20-μm thick dielectric formed on Au interconnects 10-μm thick.

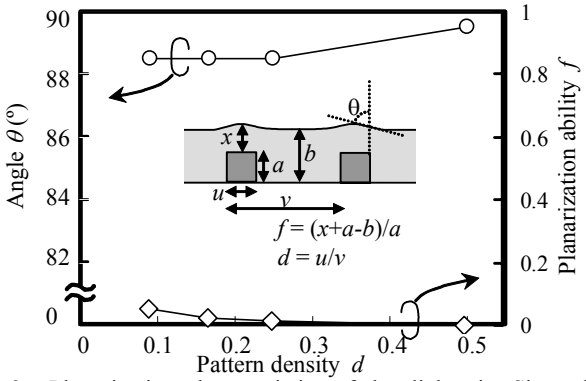

Fig. 3. Planarization characteristics of the dielectric. Since the thickness x ranges from b-$a \le x \le b$, planarization ability is 0 when the surface is completely planarized, and 1 when it is not planarized at all, by definition.

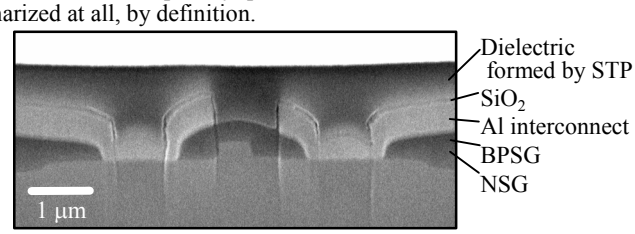

Fig. 4. FIB (focused ion beam) cross section of an n-ch MOSFET with a dielectric formed by STP. After the sample was sintered in H_2-N_2 gas at 400 ºC, the dielectric was transferred from the base film to the sample by STP and annealed at 310 ºC for 30 min.

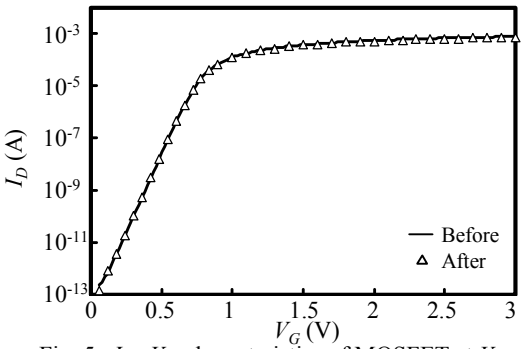

Fig. 5. I_D–V_G characteristics of MOSFET at V_D = 3 V before and after STP.

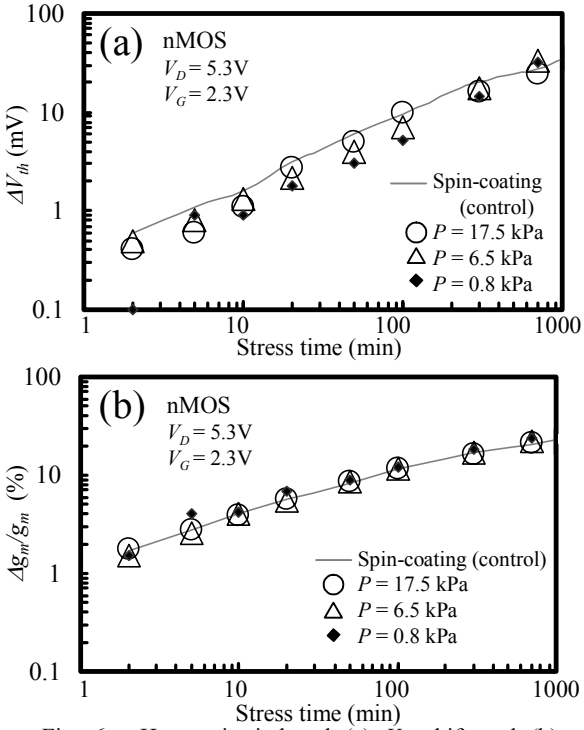

Fig. 6. Hot-carrier-induced (a) V_{th} shift and (b) g_m degradation as a function of stress time. Stress conditions were V_D = 5.3 V and V_G = 2.3 V. The temperature during hot pressing was 120 ºC.

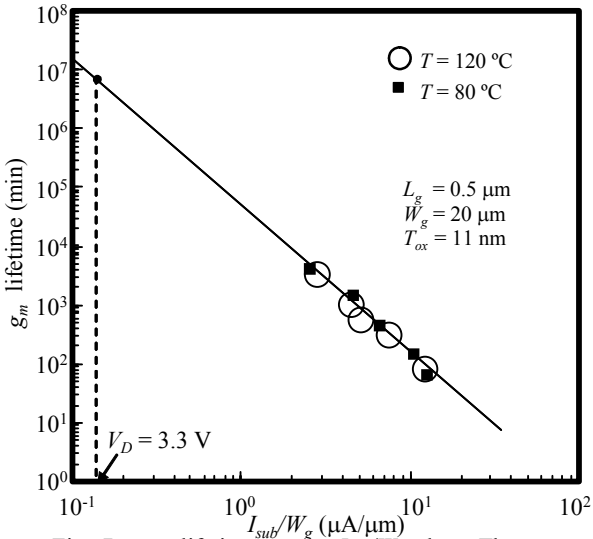

Fig. 7. g_m lifetime versus I_{sub}/W_g plots. The pressure during hot pressing was 17.5 kPa.