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High-Performance InP HBTs with a Composite Collector

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1. Introduction

Several kinds of DHBT layer structures, such as a composite collector (CC) [1], step-graded (SG) collector [2], and type-II heterojunction collector [3], have been developed to obtain high-speed and reliable device operation. In this paper, we report a composite collector design that achieves high current density and good breakdown behavior simultaneously. The proposed structure makes use of the space charge in the collector to decrease the multiplication coefficient. Fabricated devices with a 330-nm-thick collector exhibit high-injection current of over 4 mA/μm^2 with reasonably small knee voltage. They also show flat collector *I-V* curves, f_t of over 200 GHz, and f_{max} of over 300 GHz. ECL ring oscillators constructed from these devices provide the minimum gate delay of less than 4 ps, which demonstrates the high-speed potential of the proposed collector structure.

2. Design of Composite Collector

The band diagram of the composite collector is shown in Fig. 1. The collector consists of 150-nm InGaAs and 150-nm InP. A 30-nm InGaAsP layer is sandwiched between them to suppress the possible accumulation of transit carriers at the heterointerface. Since the conduction-band discontinuity is separated from the base by the 150-nm-thick InGaAs, the effect of current blocking should be very small even under high-I_C and low-V_{CE} bias conditions. Thus, this collector structure can handle much larger current than the SG-DHBT reported in [2]. The InP in the collector is lightly *n*-type doped. This increases the capacity of the space charge stored in the collector and delays the onset of the Kirk effect.

One may suspect that increasing the InGaAs layer thickness only increases the multiplication coefficient in the composite collector. This is true at low current. However, at high current, the space charge in the collector lifts the conduction-band potential in the InGaAs section, leading to the concentration of the electric-field intensity on the wide band-gap InP. Thus, the multiplication coefficient can be improved at high current. Additionally, the space charge increases the depletion layer thickness in the InP, thereby decreasing the internal collector capacitance. This effect also plays a beneficial role in increasing f_{max} through the reduction of the internal *RC* product.

3. Device Characterization

The HBT layer structures were grown on 3-inch InP substrates by MOVPE. The InGaAs base is 40-nm thick and doped with carbon to 6x10^{19} cm^{-3}. The indium mole fraction is graded from 0.53 to 0.43 toward the emitter. The mesa-type devices were fabricated using the "base-pad isolation" technique [4] to reduce the external capacitance.

Typical collector *I-V* curves are shown in Fig. 2. The CC-HBT shows much better breakdown behavior than the SHBT fabricated for comparison. Moreover, the knee voltage is almost the same as that of the SHBT even at J_C of over 4 mA/μm^2. Figure 3 plots the measured multiplication coefficient versus current density. At low current, the multiplication coefficient is as large as nearly half that of the SHBT with a 300-nm collector. However, it decreases markedly with increasing current density, approaching the value of the SG-DHBT (with 70-nm graded layers and a 230-nm InP collector). These results support the claim that the increase in the space charge alleviates the electric-field intensity in the InGaAs section and that, at high-injection current, the multiplication coefficient is primarily determined by the impact ionization in the InP.

Figure 4 shows f_t, f_{max}, and total collector capacitance for the HBT with a 0.8-μm-wide emitter. The HBT exhibits a peak f_t of 217 GHz and a peak f_{max} of 342 GHz at J_C of 2 mA/μm^2. Figure 5 plots the internal and external collector capacitances extracted using an Agilent ADS simulator. The internal capacitance decreases from 3.0 to 1.8 fF with increasing current density from 0.25 to 2.5 mA/μm^2. This reflects the increase of depletion layer thickness in the InP due to the space charge and contributes to the high f_{max}.

To investigate the high-speed potential of the CC-HBT, we also fabricated 19-stage ECL ring oscillators using 0.8x3-μm^2 emitter devices. The ECL gate is designed to exhibit a 0.4-V logic swing at a switching current of 6 mA. As shown in Fig. 6, the fabricated IC demonstrates the minimum gate delay of 3.83 ps at 7.3 mA (corresponding to 3 mA/μm^2). This short delay time results from the large current density and small collector capacitance.

4. Conclusion

We have described the design and performance of CC-HBTs having a 40-nm base and a 330-nm collector. The HBT exhibits high current density of over 4 mA/μm^2 without current blocking effect and good on-state breakdown behavior. Further improvement of device speed is naturally expected by vertical and/or lateral scaling, while the present structure exhibits ECL-gate delay of less than 4 ps.

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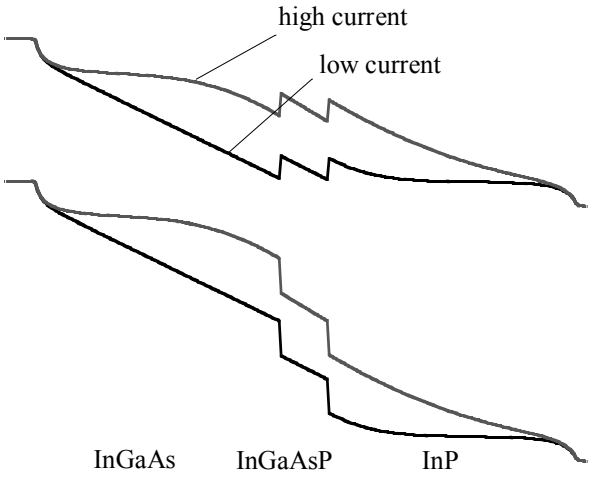

Fig. 1. Schematic energy-band diagram of the InGaAs/InGaAsP/InP composite collector proposed in this work.

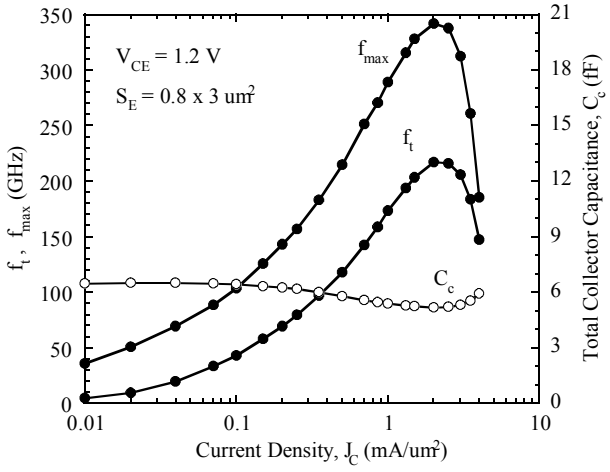

Fig. 4. f_t,f_{max} and total collector junction capacitance plotted as a function of collector current density at V_{CE} = 1.2 V.

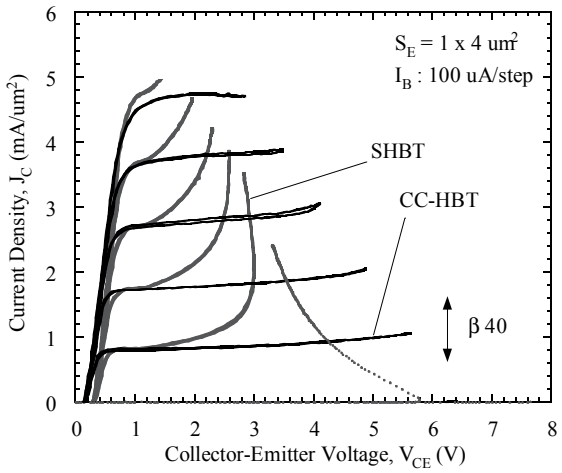

Fig. 2. Collector *I-V* characteristics. *I-V* curves for the SHBT with a 300-nm-thick collector are shown for comparison.

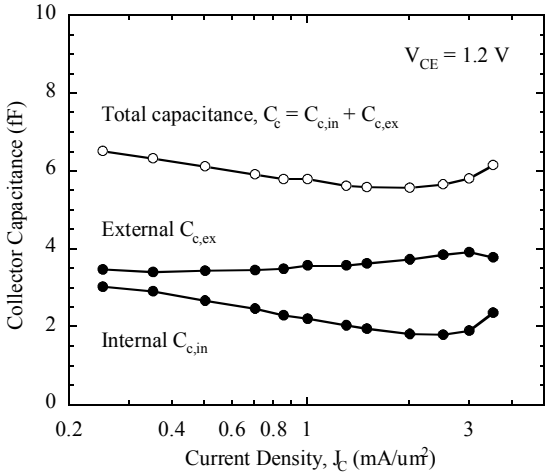

Fig. 5. Extracted internal and external collector capacitance plotted as a function of collector current density. Total capacitance is also shown.

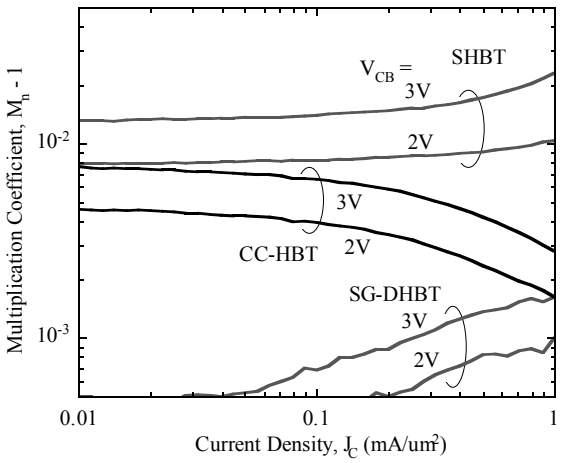

Fig. 3. Multiplication coefficient versus current density at V_{CB} = 2 and 3 V. Multiplication coefficients for the SHBT and step-graded DHBT with a 300-nm-thick collector are shown for comparison.

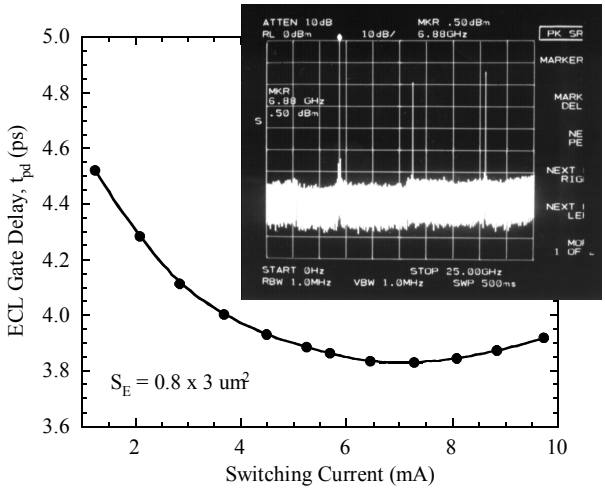

Fig. 6. ECL gate delay versus switching current. The inset shows the measured spectrum on the 19-stage ring oscillator, showing the oscillation frequency of 6.88 GHz at 7.3 mA (J_C 3 mA/μm²).