

A High Reliability and High Gain InP-HEMT with Composite Channel Structure

Shunsuke Kurachi, Yasunori Nonaka and Jun-ichiro Nikaido

Fujitsu Quantum Devices Limited

1000 Kamisukiahara, Showa-cho, Nakakoma-gun, Yamanashi 409-3883, Japan
Phone: +81-55-275-4411 Fax: +81-55-268-0244 E-mail: s.kurachi@fqd.fujitsu.com

1. INTRODUCTION

The InAlAs/InGaAs materials system offers numerous advantages which lead to the improvement of HEMT performances. Devices fabricated from InAlAs/InGaAs pHEMT currently exhibit the highest current gain cut-off frequency ($f_T = 562$ GHz for a 25-nm gate-length device) [1]. On the other hand, there are several problems such as drain conductance dispersion and poor reliability due to impact ionization in InP-based HEMTs.

We fabricated an InP-HEMT chip with a composite channel structure to suppress impact ionization and mounted it on an improved package to compensate lower transconductance. The package improves isolation of the HEMT and gain flatness for 10-18 GHz. We achieved a noise figure of 0.28 dB and an associated gain of 16.5 dB at 12 GHz for a 200- μ m gate-width. To our knowledge this is the highest associated gain at 12 GHz with high reliability.

2. DEVICE FABRICATION

Figure 1 shows a cross sectional view of our InAlAs/InGaAs HEMTs, grown by MOCVD on 3-inch semi-insulating InP wafers. Each layer is lattice-matched to the InP substrate except for an InGaAs channel layer. We improved the uniformity of threshold voltage by growing an InP etch-stopper layer on the InAlAs carrier supply layer. We also adopted pseudomorphic structure for the InGaAs channel layer to improve reliability. It is well known that the poor reliability problem is closely related to impact ionization in the InGaAs channel that has a narrow band-gap. Several researchers have reported ways to suppress impact ionization [2,3]. We adopted composite channel layer that consists of an upper $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer and a lower $\text{In}_{0.35}\text{Ga}_{0.65}\text{As}$ layer to suppress impact ionization. We think that the mole fraction variation of InGaAs is more stable and reproducible method to grow high mobility composite channel by MOCVD.

We formed both a gate electrode and a gate recess by using electron-beam lithography, and used selective wet chemical etching for fabricating the recess structure. The InP surface at the recess region was covered with a thin SiN dielectric film grown by plasma CVD [4]. The gate electrode consisting of Ti/Pt/Au was evaporated onto the InP layer and lifted off. The gate length was typically 0.13 μ m. The devices were fully passivated with SiN, and upon completion of front-side processing, wafers were thinned to a thickness of 140 μ m. The discrete InP-HEMT chip was mounted on a

70-mil surface mount type of ceramic package. A thin metal layer connected to the ground was inserted into the ceramic wall of the package. Then the ceramic wall height was optimized to improve isolation. We call this metal layer a seal ring and evaluated the chip performance with and without the seal ring.

3. RESULTS AND DISCUSSIONS

Figure 2 shows the current-voltage characteristics of the developed HEMT with a 200- μ m gate-width measured at room temperature. The transconductance (g_m) was 805 mS/mm. This value was, however, lower than reported results (for example, 917 mS/mm for conventional channel structure [4]).

Figure 3 shows the frequency dependence of maximum stable gain (MSG) of the HEMT with and without the seal ring under the following measurement conditions: $V_{DS} = 1$ V and $I_{DS} = 50$ mA/mm. It indicated that the HEMT with the seal ring package exhibits better gain flatness for 10-18 GHz due to improvement of isolation.

We measured noise performance of the HEMTs with the seal ring package at 12 GHz. Fig. 4 shows the drain current dependence of the noise figure and the associated gain at room temperature. The noise figure of 0.28 dB and the associated gain of 16.5 dB were achieved for a drain-source current (I_{DS}) of 75 mA/mm.

We confirmed reliability performance under the following accelerated life test condition: $V_{DS} = 1.5$ V and $I_{DS} = 150$ mA/mm at 175°C in nitrogen ambient. Fig. 5 shows the comparison of transconductance degradation rate for the fabricated conventional and composite channel HEMTs. After 2000 hours at 175°C, the g_m degraded by only 4%. We believe that the good result for high reliability is due to suppression of impact ionization by using composite channel structure.

4. CONCLUSION

We fabricated the InP-HEMT with the composite channel structure and the seal ring package. The HEMT exhibits better gain flatness for 10-18 GHz. Its g_m degradation during reliability test at 175°C is almost negligible. This result emphasizes that InP-based HEMT with the composite channel structure is essential for high reliability.

ACKNOWLEDGEMENTS

The authors would like to thank Y. Tateno and Y. Mimino for their helpful discussions throughout this work. We also wish to thank H. Kawata and S. Takase for their encouragement.

Source	Gate	Drain
n+-In _{0.53} Ga _{0.47} As		contact layer
i-InP		stopper layer
i-In _{0.52} Al _{0.48} As		barrier layer
n+-In _{0.52} Al _{0.48} As		supply layer
i-In _{0.53} Ga _{0.47} As		channel layer
i-In _{0.35} Ga _{0.65} As		buffer layer
i-In _{0.52} Al _{0.48} As		buffer layer
		S.I.InP sub.

Fig. 1 Cross sectional view of our HEMTs.

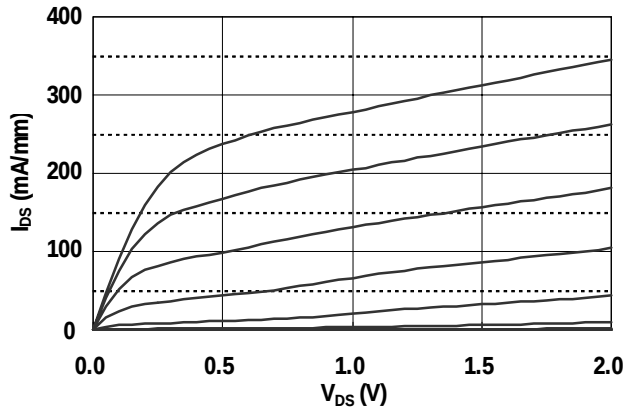


Fig. 2 DC I-V characteristic of our HEMTs. (Gate voltage maximum is 0 V and gate voltage step is 0.1 V.)

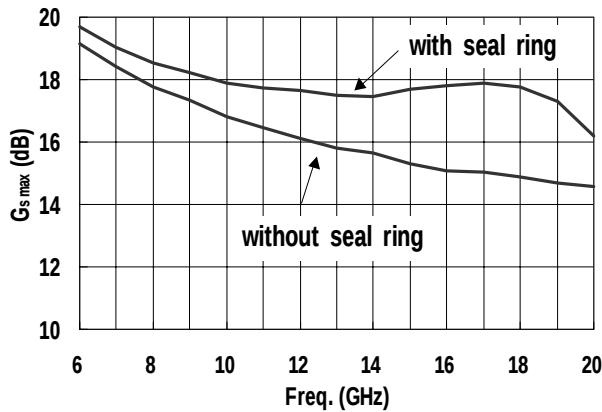


Fig. 3 The frequency dependence of maximum stable gain (MSG) of our HEMTs with and without the seal ring. ($V_{DS} = 1$ V, $I_{DS} = 50$ mA/mm)

REFERENCES

- [1] Y. Yamashita *et al.*, *IEEE Electron Device Letters* **EDL-23**, (2002) p.573
- [2] N. Okamoto *et al.*, *IEDM Digest 2001*, p. 189
- [3] K. Sawada *et al.*, *IEEE Trans. Electron Devices* **ED-50**, (2003) P. 310
- [4] T. Takahashi *et al.*, *Proceedings of 2001 IPRM*, p. 614

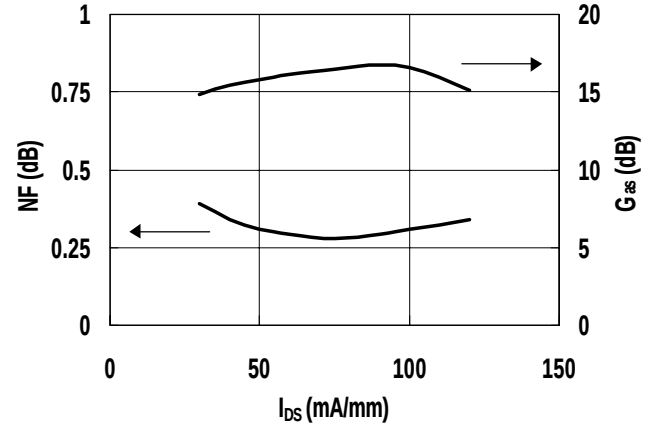


Fig. 4 Drain current dependence of the noise figure and the associated gain.

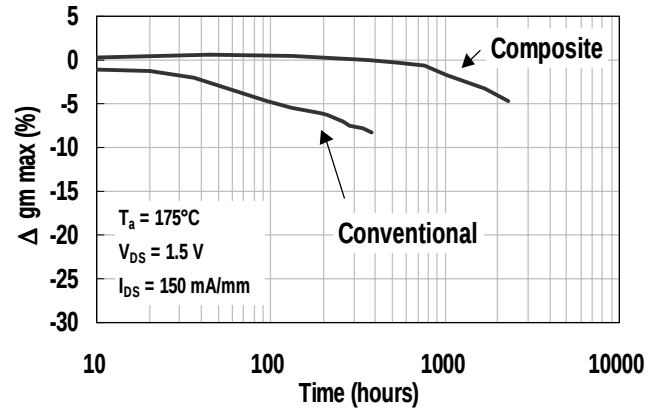


Fig. 5 Comparison of transconductance degradation rate for conventional and composite channel structure.