Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 902-903

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75-GHz Optical Clock Divide-by-Two OEIC using InP HEMTs and Uni-Traveling-Carrier Photodiode

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1. Introduction

Ultra-fast ICs operating at 40 Gbit/s and beyond are being studied and developed for application to optical fiber communications system and measurement instruments. To ensure such ultra-fast operation, a wide bandwidth of interconnections to the IC chips as well as a fast operating speed inside the chips is necessary. From this viewpoint, optoelectronic ICs (OEICs) that monolithically integrate photodiodes and electrical devices are attractive to widen the bandwidth because broadband optical interconnections can be used. In the range of 40-80 Gbit/s, not only conventional analog OEICs, such as preamplifiers with photodiodes [1][2], but also digital ones, such as delayed flip-flops [3][4], have been demonstrated. In the OEICs, the requirement for 50-Ω impedance matching between photodiodes and electrical circuits is greatly relaxed because commonly used 50-Ω components, such as cables and connectors, are not needed. This means that new circuit configurations that are not limited by 50-Ω systems become possible.

In this paper, we describe optical clock divide-by-two OEICs based on a new circuit configuration. The configurations utilize the merits of the monolithic integration of photodiodes and transistors. Using a process integrating InP HEMTs and uni-traveling-carrier photodiodes (UTC-PDs), the OEICs were fabricated and confirmed to operate up to 75 GHz.

2. Circuit Design

Figure 1(a) is a block diagram of the ICs. The ICs consist of three blocks: an optical-clock-driven toggle flip-flop (O-CK TFF), a buffer amplifier, and a 50-Ω driver. O-CK TFF is the core circuit that has a function of divide-by-two by itself. We designed two types of O-CK TFF, which are shown in Fig. 1(b) and (c). Type-I [Fig. 1(b)] is based on a clocked inverter TFF [5], where one of the lower-level differential pair transistors is replaced by a UTC-PD. A UTC-PD can output sufficient photocurrent even in a low-bias condition [6]. Therefore, the current through the upper-level differential pairs can be switched, and divide-by-two operation can be attained. Also, monolithic integration is indispensable for the type-I configuration, because neither the anode nor cathode side of the UTC-PD matches 50 Ω. Type-II [Fig. 1(c)] consists of a differential electrical clock generator (DECG), passive level shifter (PLS), and conventional clocked inverter TFF. In the DECG, two 50-Ω resistors are connected at the anode and cathode of the UTC-PD, respectively. The resistors work in conjunction with the photocurrent, causing the voltage level of the anode to rise and that of the cathode to fall, so that differential signal is generated. The PLS adjusts the bias level of the differential signal so that the lower-level differential pair in the TFF can operate at a proper bias level. Also in Type-II, monolithic integration is preferable to a hybrid approach, because 180°-phase difference in the differential signal is easy to maintain due to the small variation of line lengths. The buffer amplifier and the 50-Ω driver are differential amplifiers based on source-coupled FET logic circuitry (SCFL). The buffer amplifier includes inductors connected to load resisters in series to enhance the bandwidth. The 50-Ω driver is an open-drain type and equipped with 70-Ω back-terminated resistors.

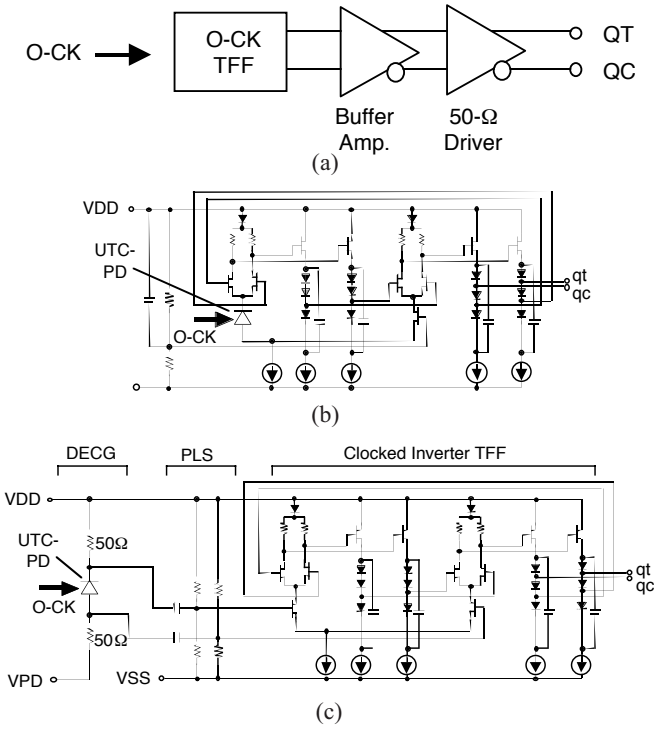

Figure1. Circuit block diagrams of the optical clock divide-by-two OEIC.
(a) Block diagram of the divide-by-two OEICs.
(b) Optical clock TFF (type-I). (c) Optical clock TFF (type-II).

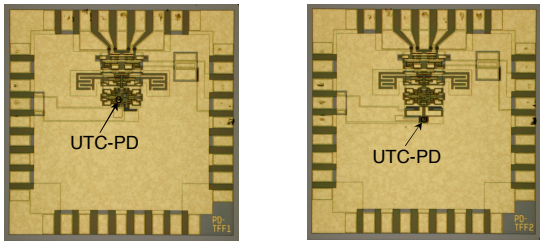

Figure 2. Chip photographs of the fabricated OEICs.
(a) Type-I. (b) Type-II (Both chip : 2 mm x 2 mm).

3. Fabrication

On a 3-inch InP wafer, the epitaxial layers of the HEMTs, Schottky diodes, and UTC-PDs were stacked in that order by MOCVD method. Then, UTC-PD, Schottky diode, and 0.1-μm gate-length InP HEMT processes were carried out [7]. The transconductance (g_m), current cutoff frequency (f_T), and threshold voltage (V_{th}) of the HEMTs are 1.1 S/mm, 164 GHz, and -730 mV, respectively. For the UTC-PD, the bandwidth was estimated to be 115 GHz, and responsivity of 0.2 A/W was measured. Figure 2 is a chip photograph of the fabricated OEICs. The chip size is 2 mm x 2 mm for both types of OEIC.

4. Measurement Results

The OEICs were measured on wafer. The input optical clock was generated by an in-house optical pulse generator [8] that can output 10-80-GHz repetition-rate optical pulses by means of electro-optic phase modulation, linear chirp compensation, and optical time-division multiplexing techniques. The generated optical clock was input from the backside of the wafer. Output electrical signals (QT, QC) were fed to a spectrum analyzer and a sampling oscilloscope, respectively.

Figure 3 shows the operating waveforms and output spectra at the maximum operating speed. Type-I and type-II operated for the 75- and 70-GHz optical clock with the average input power of +15.8 and +14.8 dBm, respectively. Here, the observed optical clock waveforms were slightly degraded, which seems to be due to the limited bandwidth of the sampling oscilloscope (50 GHz). The output signals for both types have > 700 -mVpp amplitude and frequency components of half the input clock rates. In the range of 0-50 GHz, we confirmed that there were no frequency components except those for half the input clock rate. The power consumptions were 1.14 W (type-I) and 1.20 W (type-II) at a supply voltage of -5.2V. Figure 4 shows the input sensitivity against the input frequency for both OEICs. The most differentiating feature is that the type-II has a self-oscillation at 68.5GHz, whereas the type-I does not in principle. This leads to a superior input sensitivity of type-II, especially around the self-oscillation frequency.

5. Conclusion

The optical clock divide-by-two OEICs, which have new circuit configurations taking advantage of monolithic integration, have been described. The OEICs were fabricated by integrating InP HEMTs and UTC-PDs. They operate at up to 75 GHz. This shows the high potential of the new configuration for OEICs beyond 40 Gbit/s.

Acknowledgment

The authors thank M. Muraguchi, J. Yumoto, H. Toba, and K. Komatsu for their encouragement during this work.

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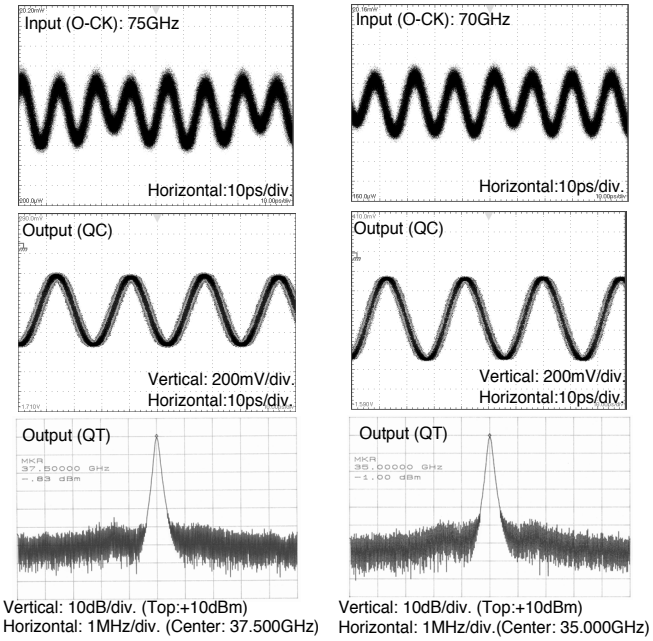

(a) (b)

Figure 3. Operating waveforms (upper and middle) and output spectra (lower) of the divide-by two ICs.
(a) Type-I at 75 GHz. (b) Type-II at 70 GHz.

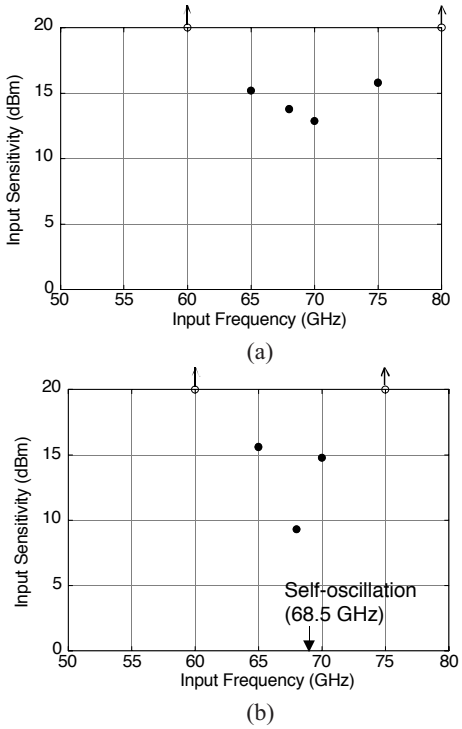

Figure 4. Measured input sensitivity against input frequency.
(a) Type-I. (b) Type-II.

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