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High-Speed III-V HEMT and HBT Devices and Circuits for ETDM Transmission beyond 80 Gbit/s

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1. Introduction

This work presents an overview of the current status on devices and circuits for electronic time division multiplexing (ETDM) applications with data rates beyond 80 Gbit/s. This paper covers mainly III-V based approaches and highlights the current state-of-the-art, especially with respect to the activities in Europe and with a glimpse on Si(Ge) results.
Several device technologies are currently compeeting for high-speed low-power applications at and beyond 80 Gbit/s. These include conventional InP based (D)HBTs [1], InAlAs/InGaAs HEMTs [2], GaAsSb based HBTs [3], and SiGe HBTs [4,5]. Fig. 1 gives an overview of the evolution of the cut-off frequencies of both SiGe and InP HBT technologies over time. It can be seen, that speed levels beyond 300 GHz are within reach by an increasing number of both III-V and SiGe HBT technologies. In Europe, Infineon [5] showed strong activities towards SiGe HBT [5]. Former Opto+, now Alcatel, demonstrated initial results for 80 Gbit/s operation [9].

2. Frequency Dividers and Ring Oscillators

Both HEMT and HBT static dividers have been published suitable for circuit operation at or beyond 100 Gbit/s [6,7]. Fig. 2 gives the input sensitivity curves for a 2:1 static (up to 66 GHz) and a 2:1 dynamic frequency divider in the W-band up to 108 GHz. The chip image of the dynamic divider is given in Fig. 3. The dividers are based on metamorphic InAlAs/InGaAs technology on 4 inch GaAs with a gate lengths of 100 nm similar to the technology in [6]. Recent progress of ring oscillators yields gate delay times of 2.0 ps per stage in InP HBT technology in [8].

3. Multiplexers and Demultiplexers

Several selector type multiplexer circuits have been published suitable for >80 Gbit/s operation: In [2], a 100 Gbit/s selector circuit is demonstrated based on InP HEMT technology from NTT. In [9], a similar circuit is given based on InP DHBT technology from Alcatel. Our own HEMT based MUX activities so far yielded on-wafer operation at 70 Gbit/s. Based on recent InP DHBT activities at Fraunhofer IAF, Fig. 4 shows the eye diagram of a 2:1 MUX core at 50 Gbit/. For the receiver side, Fig. 5 gives the chip image of 1:2 demultiplexer based on 100 nm HEMT technology with about 270 active transistors. Fig. 6 gives the output signal of channel 1 of the HEMT demultiplexer at an input signal of 80 Gbit/s.

4. Driver Circuits

For applications beyond 80 Gbit/s, both InP HEMT and HBT circuits are currently considered. GaAsSb HBTs [3] promise even more output voltage swing at increased speed beyond 100 GHz. A concise overview of the various activities is given in the full paper.

5. Conclusions and Acknowledgements

Despite of the ongoing baisse of the telecom industry, devices and circuits for data rates beyond 80 Gbit/s see strong progress based on both SiGe and III-V semiconductor technologies.
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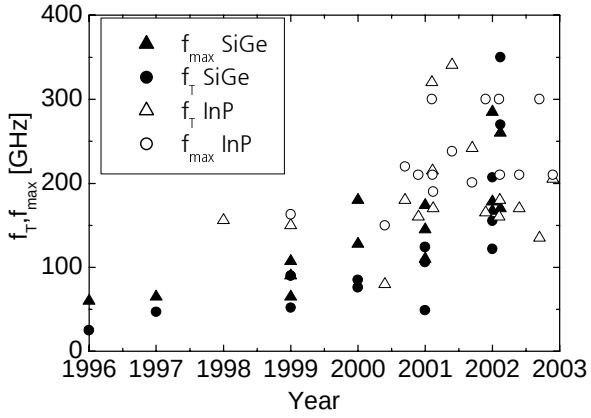

Fig. 1: Cut-off frequencies f_T and f_{max} over time for SiGe and InP HBTs.

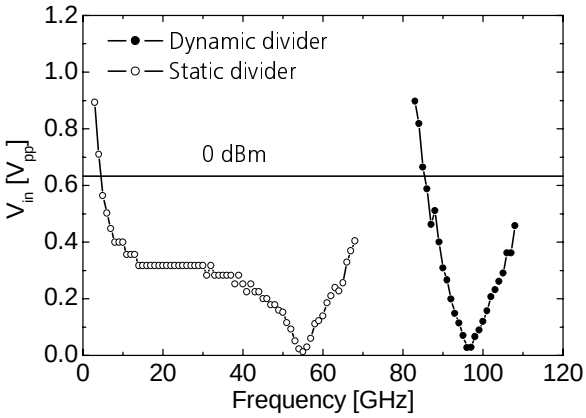

Fig. 2: Input sensitivity of a static and dynamic frequency divider based on 100 nm metamorphic HEMT technology.

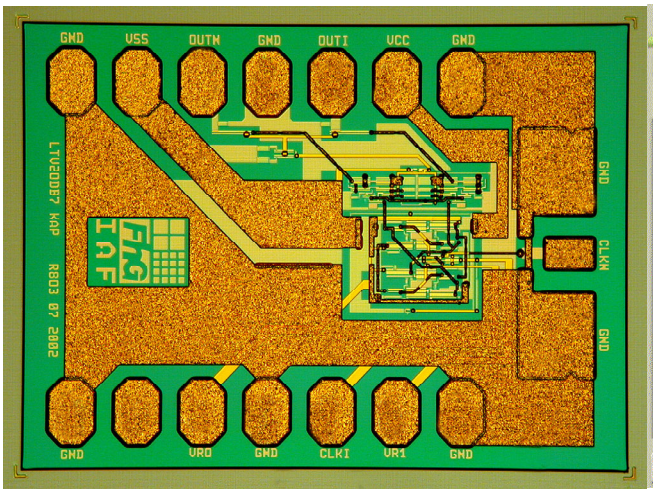

Fig. 3: 108 GHz 2:1 dynamic frequency divider based on 100 nm metamorphic HEMT technology.

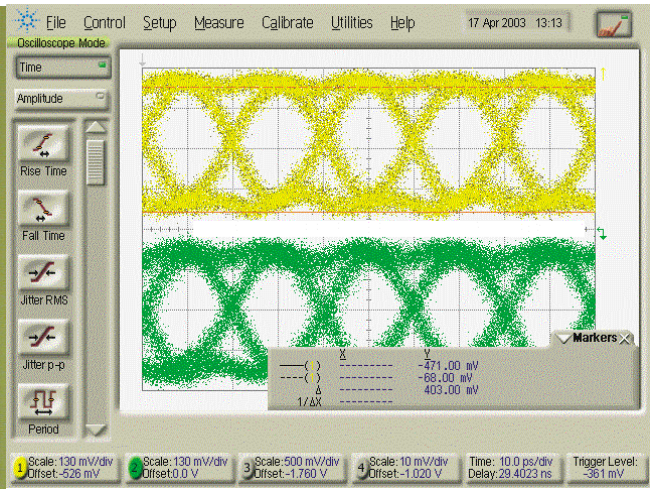

Fig. 4: Eye diagram of a 50 Gbit/s InP DHBT multiplexer core.

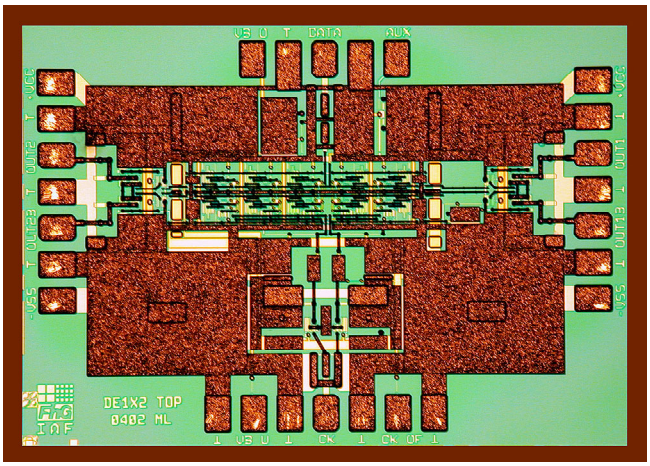

Fig. 5: Chip image of a 1:2 demultiplexer with a chip area of 1.75 mm×1.25 mm based on MHEMT technology.

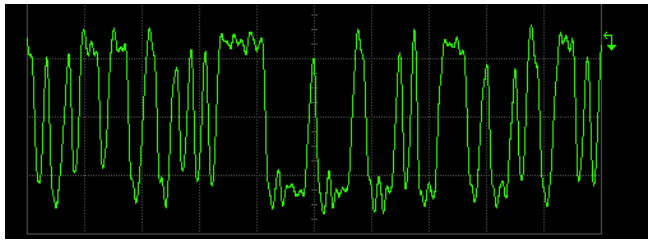

Fig.6: Output signal of channel 1 at 80 Gbit/s input signal of the demultiplexer based on 100 nm MHEMT technology.