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All digital One- chip Wireless Modem LSI with Acquisition Circuit

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1. Introduction

Radio frequency identification (RF-ID) is one of significant wireless technologies for ubiquitous network. Requirements of RF-ID are ultra-small package, low power operation and low cost implementation. μ-chip [1], which has been proposed and fabricated by Hitachi Ltd., is ultra-small RF-ID chip. The μ-chip was designed using analog/digital mixed signal process. The μ-chip doesn't have a function of interactive communication.

We have already proposed all digital one-chip modem with the size of 150μm x 150μm [2]. The modem is designed only using digital CMOS logic gate.

In this paper, we have designed acquisition circuit for frequency offset, in order to achieve full_duplex communication. Media access control circuit has been designed.

2. New design method of the All Digital Modem

A feature of proposed modem is to be designed of digital logic gate. Figure 1(a) shows BPSK modulator using a clock divider, differential encoder and an exclusive-OR (ex-OR) component. We can design the modulator only 4 flip-flops and some peripheral logic gate. Figure 1(b) shows BPSK demodulator. Received signal is converted to 1-bit digital signal including carrier wave using CMOS amplifier. Received signal is demodulated by differential detection using a delay line and ex-OR component. Demodulated data is obtained through a low pass filter (LPF) for signal shaping.

Figure 2 shows measurement result of bit error rate (BER) performance of proposed modem. In this measurement, synchronization between transmitter and receiver is ideal. System parameter is listed in Table.1. Field Programmable Gate Array (FPGA) was used for implementation. As shown in Fig.2, degradation at BER of 10^{-3} is less than 0.5dB from theoretical value.

3. Design of acquisition circuit

Since frequency offset usually exists between transmitter and receiver in wireless communication. It is necessary to design acquisition circuit for all digital modem. In the receiver, three kind of synchronization is needed for demodulation, As shown in Fig.2. The first acquisition is carrier synchronization. It means sampling clock (sam_clk) synchronization after 1-bit conversion. Sampling clock is used in order to perform differential detection. The second acquisition is symbol synchronization. It means data clock (data_clock) synchronization after differential detection. Data clock is used for a data decision. The Third acquisition is frame synchronization. It means frame clock synchronization. Frame clock is used in order to extract information from packet frame correctly and to perform error detection. We designed packet frame component. Figure 4 shows the packet format. Size of 1 packet is decided as 240 bits. For acquisition of sampling clock, 4-bit ramp bits are inserted into the top of packet. For acquisition of data clock, 8-bit preamble bits are inserted. Preamble pattern is "10101010". Symbol acquisition is established using zero cross detection at the border of symbol. For frame acquisition, 16-bit unique word (UW) is placed after preamble. Information block is 180 bits. Cyclic redundancy check (CRC) for error detection is 16 bits. Acquisition circuit was designed as shown in Fig.5.

Frame error performance depending on frequency offset between transmitter and receiver was measured using FPGA. Figure 6 shows the measurement block diagram. Frequency offset is given as frequency difference of system clock. Figure 7 shows standardized frame error rate as a function of frequency offset. Frame error rate is less than 10^{-6} at the frequency offset of 12ppm. Since frequency stability of commercially available crystal oscillator for wireless communication is less than 3ppm, it is confirmed that the designed circuit has sufficient performance for practical use.

4. ASIC fabrication and evaluation

The all digital modem has been fabricated using 0.18μm CMOS process. We used CMP (Circuit Multi-Projets, France) as a broker and STMicroelectronics as a foundry. Figure.8 shows the photograph of fabricated modem. Size of this modem is 147μm x 140μm.

We have evaluated operation frequency of transmitter. The measured maximum operation frequency was 800MHz. The clock frequency of 800 MHz provides 100MHz carrier frequency and 25Mbit/sec data rate.

5. Conclusion

We have proposed the all digital wireless modem. A proposed new modem has synchronization acquisition circuit. We show that this modem has a high data rate and a small chip size. A proposed chip has a potential for being used to short-range communication, such as RF-ID and in vivo communication.

Acknowledgement

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References

[1] K.Takaragi, et al., "An Ultra Small Individual Recognition Security Chip," IEEE Micro, vol.21, no.6, pp.43-49, Nov/dec. 2001.

[2] H.Nakase, et.al, "All Digital Wireless Modem LSI for Software Defined Radio," SSDM2001, (2001) pp.406-407.

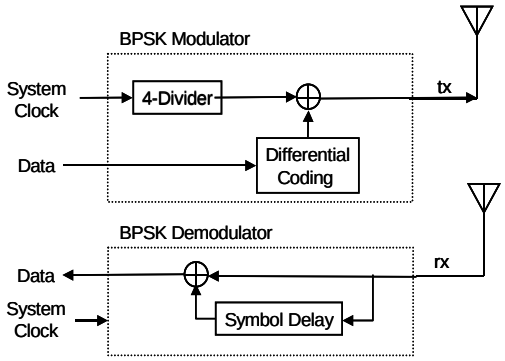

Fig.1 (a) BPSK Modulator Circuit (b) BPSK Demodulator Circuit.

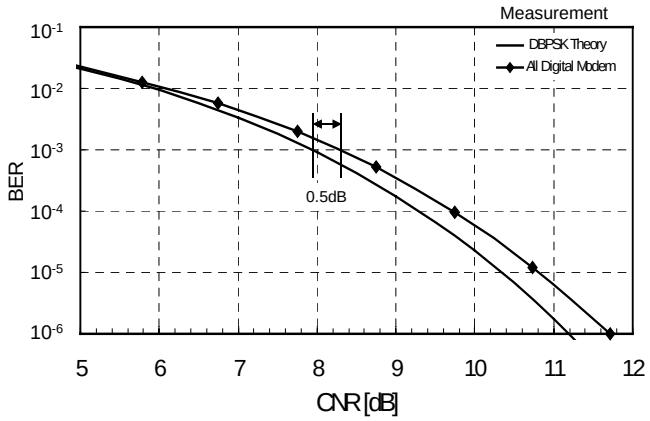

Fig.2 BER Performance of BPSK Modem.

Table.1 Measurement Parameter.

Modulator&Demodulator Parameter	
Clock Freq	84 MHz
Carrier Freq	21 MHz
Symbol Rate	5.25 Msps
Detection Technique	Differential Detection

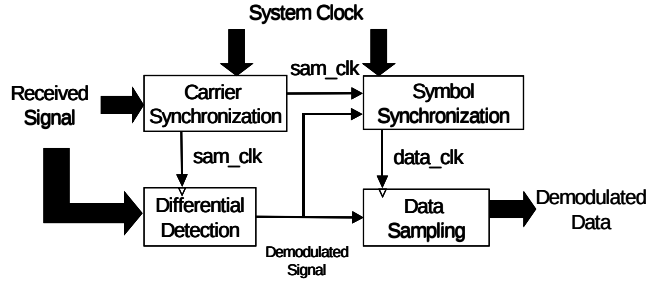

Fig.3 System Structure of Delimited BPSK Receiver.

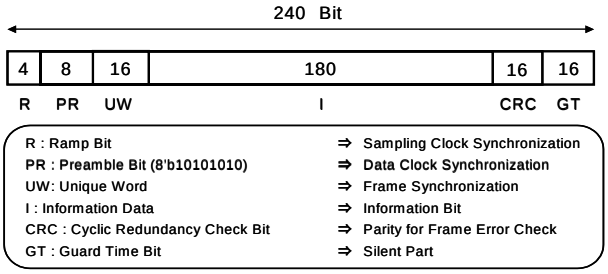

Fig.4 Frame Structure.

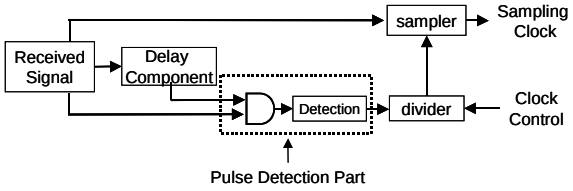

Fig.5 Acquisition Circuit for sampling clock .

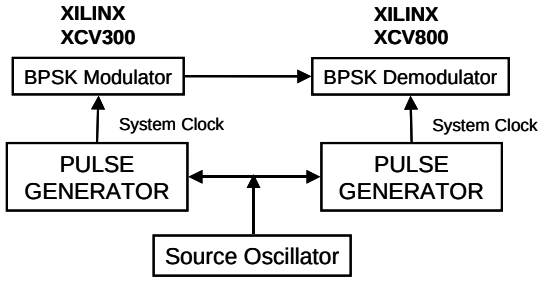

Fig.6 Measurement block diagram of Frame Error Rate

Fig.7 Frame Error Rate .

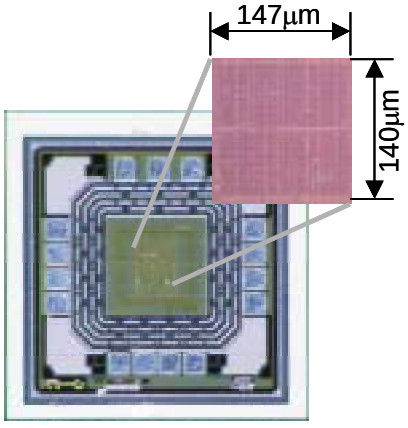

Fig.8 Photograph of all digital modem.