Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 640-641

P10-1

Improvement of Data Retention in Floating Gate Flash EEPROM's with P-Doped Floating Gate

B. C. Wu[1], H. W. Tsai[1], S. S. Chung[1], C. J. Lin[2], D. S. Kuo[3], and M. S. Liang[2]
[1]*Department of Electronic Engineering, National Chiao Tung University, Taiwan*
[2]*Tsmc, Science-based Industrial Park, Hsinchu, Taiwan* [3]*Nexflash Inc., San Jose, U.S.A.*

Abstract- Data retention capability is the key to design a highly reliable non-volatile memory cell. We demonstrated in our previous work [1] that the use of p-type floating gate(FG), instead of the commonly used n-type doped FG in an n-channel cell, is feasible for high speed performance as well as better endurance. In this paper, a p-doped floating gate on both n- and p-channel flash cells can be achieved with superior data retention characteristics. Since the p-floating gate cell exhibits a larger tunnel oxide field and a smaller electric field across the ONO dielectric during programming, the p-type FG cell shows much better charge loss behavior as compared to n-type FG ones. Results have been demonstrated for both n- and p-channel flash cells. Along with the high speed, better disturb, and good endurance advantages, the p-type FG cell is very promising for high performance and high reliability applications.

Device Preparation

The cells used in this study are ETOX n- and p-channel flash memory (Fig. 1), fabricated using 0.35um triple well technology. The thickness of the tunnel oxide is 90Å. The floating-gate dopants are split into in-situ doping with Phosphorus (n-type), undoped, medium, and high dopant with Boron (p-type) as given in Table 1. The interpoly dielectric of ONO structure is formed with an equivalent thickness of 165Å. In addition, the dummy cells with connected floating- and control gates, are also used for measurements. For P/E cycling, channel hot electron is used for programming of n-channel cells, BBHE[2] is used for programming of p-channel cells, while erase of both cells is made by channel FN.

Results and Discussion

A. Comparison of the ONO Electric Fields

To verify the electric field across the tunnel dielectric, the FN tunneling measurement is performed for dummy cell. Fig. 2 shows the results, where we see that p-type FG cell has larger gate current. This reveals that the tunnel oxide(TO) electric field is larger for p-type FG cell. Under the same gate-to-substrate voltage drop, since tunnel oxide field is larger in p-type FG cell, the ONO field in p-type FG cell becomes smaller. The equations in Table 2 are used to explain why the ONO field is smaller in a p-type FG cell. Under the same applied voltage, p-type floating-gate cell has larger V_{FG}. So, the ONO dielectric field of p-type FG cell is smaller than n-type ones. This can also be illustrated in Fig. 3 with a comparison of the band diagrams for n-type and p-type FG. The reduction of charge loss in the p-type FG cell can be attributed to a smaller ONO dielectric field as explained below.

B. Charge Loss Characteristics for N-channel Cells

Fig. 4 shows the threshold voltage shift versus temperature as well as the dopant effect. It was found that the flash cell with higher p-type concentration has lower V_{TH} shift. The higher concentration of the p-type floating-gate, the lower the charge loss is. In other words, the cell with higher p-type FG doping concentration exhibits much better characteristics. In addition, Fig. 5 shows the charge loss characteristics of n-channel cells before and after P/E cycling. It is concluded that not only the floating-gate dopant type but also the doping concentration will affect the charge loss characteristics.

C. Gate-Disturb and the Leakage Mechanism

The charge loss may be caused by two paths, one is the trap of electrons in the nitride layer, and the other one is the generated damage in the tunnel oxide, after long term P/E cycles [3]. To verify the low charge loss in p-type FG cell, gate-disturb and the SILC have been plotted in Figs. 6 and 7. The gate-disturb of flash cells before and after cycling at high oxide field is shown in Fig. 6, where the p-type FG cell has better disturb characteristics than the n-type ones. This implies that less oxide damage generated during the P/E cycles. Fig. 7 shows the time evolution of ΔQ_{FG}. The n-type FG cell has large charge loss rate. Furthermore, leakage current due to trap-assisted tunneling can be obtained from $-\Delta Q_{FG}/\Delta t$. Apparently, much less leakage is observed in p-type FG cell as a result of smaller oxide traps in the tunnel oxide and a lower ONO field as mentioned above.

D. Charge Loss Characteristics for P-channel Cells

Fig. 8 shows the charge loss characteristics for p-channel cells with different floating-gate types before and after P/E cycling operations, at a baking temperature of 250°C. Obviously, the p-type one has better charge loss behavior which can be explained with the same reason as for n-channel cells. The p-type FG exhibits much better gate disturb characteristics (not shown here), less defects and traps were generated during P/E cycling. As expected, p-type FG has better charge loss characteristics. One most exciting result is shown in Fig. 9. The p-channel flash cell has an inherent disadvantage of poor drain-disturb [4] since its introduction in [5], while the use of p-type FG can solve the problem, as shown in Fig. 9, with a 3-order of drain-disturb improvement. The reason of this improvement is revealed in Fig. 10, which shows the gate currents for different floating-gate. Drain disturb is determined by BTB(Band-To-Band) tunneling when the cell is in programmed state, and by CHH(Channel Hot Hole) tunneling when the cell is in erased state. Obviously, the n-type one has larger CHH currents than the p-type one. This can explain why the p-type FG cell has better drain disturb characteristics.

In summary, the p-type floating-gate flash cell has much lower electric field in the ONO dielectric layer and a smaller gate-disturb by comparing with that of conventional n-type FG during programming. Therefore, fewer traps in the ONO layer and tunnel oxide were generated. This is the reason why p-type FG has much better charge loss characteristics. Also, we have seen a 3-order improvement of the drain-disturb in p-type FG p-channel cells. Along with the high speed, better disturb, and good endurance advantages, the p-type FG cell is useful and promising for high performance and high reliability applications in both n- and p-channel cells.

Acknowledgments This work was supported by the National Science Council, Taiwan, under grant NSC89-2218-E009-110 and in part by the Tsmc, R&D division, Taiwan.

References

[1] S. S. Chung et at., in ***Symp. on VLSI Technology***, p. 19, 1999.
[2] T. Ohnakado et al., in ***IEDM Tech. Digest***, p. 279, 1995.
[3] S. S. Chung et al., in ***IEEE Trans. ED.***, vol. 48, No. 3, p. 300, 2001.
[4] S. S. Chung et al., ***Proc. IRPS***, Orlando, p. 67, 2001.
[5] C. C.-H. Hsu et al., ***Extended Abs. SSDM***, p. 140, 1992.

	U	P-	P+	N+
T_{ox}(Å)	90			
T_{ono}(Å)	T.O/Si_3N_4/B.O=65/90/55			
Floating Gate Doping	undoped	BF_2 20Kev 1E13	BF_2 20Kev 5E13	In-situ

Table 1 The split conditions of floating gate for both n- and p-channel cells used in this study. The masked length L= 0.65um and width W= 0.7um).

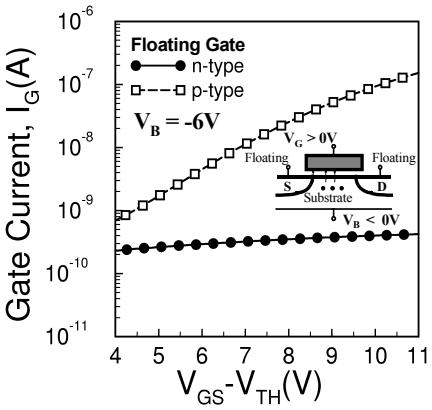

Fig. 2 Measured channel Fowler-Nordheim (FN) tunneling currents for dummy cells with n- and p-type doped floating-gates. A larger I_G in p-type FG exhibits a larger tunnel oxide field.

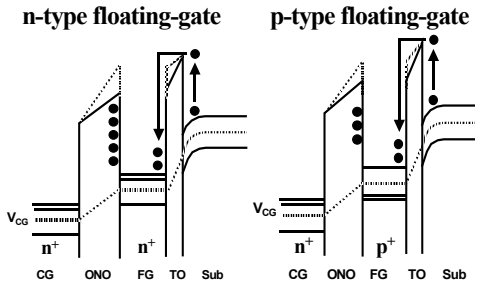

Fig. 3 The energy band diagrams for n-type and p-type floating gate n-channel cells during programming. Note that p-type FG has larger tunnel oxide field and smaller ONO field.

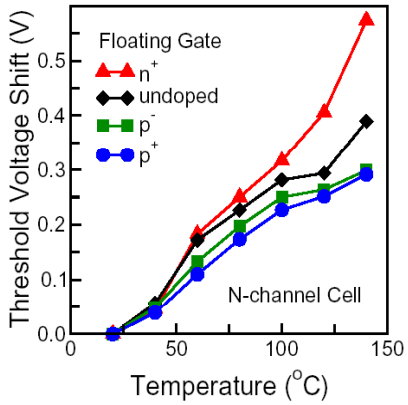

Fig. 4 Comparison of threshold voltage shift versus temperature for different floating-gate dopant types and doping concentrations.

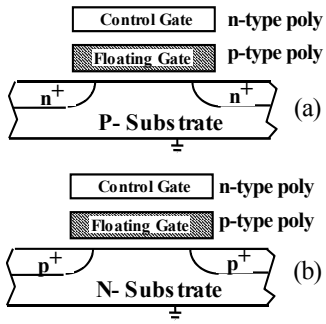

Fig. 1 The experimental p-doped floating gate flash cells: (a) n-channel and (b) p-channel cells. Control samples with n-doped floating gate were also made for comparison.

$$Q_{FG} = C_{CG}(\Psi_{FG}-\Psi_{CG}) + C_S(\Psi_{FG}-\Psi_S) + C_D(\Psi_{FG}-\Psi_D) + C_B(\Psi_{FG}-\Psi_B) \quad (1)$$

$$\Psi_{FG} = \frac{C_{CG}}{C_{TOT}}\Psi_{CG} + \frac{C_S}{C_{TOT}}\Psi_S + \frac{C_D}{C_{TOT}}\Psi_D + \frac{C_B}{C_{TOT}}\Psi_B + \frac{Q_{FG}}{C_{TOT}} \quad (2)$$

For n-type floating-gate :

$$V_{FG} + \Psi_{FG} = \alpha_{CG}(V_{CG} + \psi_{CG}) + \alpha_D(V_D + \psi_D) - \frac{Q_{FG}}{C_{TOT}} + \alpha_S\Psi_S + \alpha_B\Psi_B \quad (3)$$

For p-type floating-gate :

$$V_{FG} - \Psi_{FG} = \alpha_{CG}(V_{CG} + \psi_{CG}) + \alpha_D(V_D + \psi_D) - \frac{Q_{FG}}{C_{TOT}} + \alpha_S\Psi_S + \alpha_B\Psi_B \quad (4)$$

Also, $V_{FG(n)} < V_{FG(p)}$ (always)

During Programming ⇨ $V_{TO(n)} < V_{TO(p)}$, $V_{ONO(n)} > V_{ONO(p)}$

During erase ⇨ $V_{TO(n)} > V_{TO(p)}$, $V_{ONO(n)} < V_{ONO(p)}$

Table 2 The equations used to calculate the electric field of ONO inter-poly dielectric.

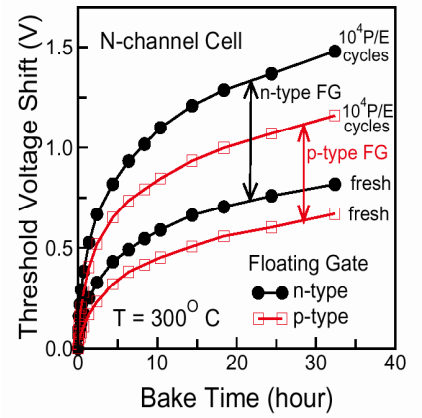

Fig. 5 The charge loss (expressed in ΔV_{TH}) for the n-channel flash memory cells with n- and p-type doped floating-gate at 300°C.

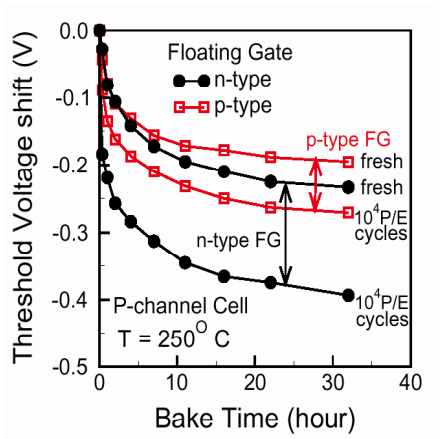

Fig. 8 Charge loss characteristics of p-channel cells with n- and p-type FG before and after 10^4 P/E cycles at 250°C.

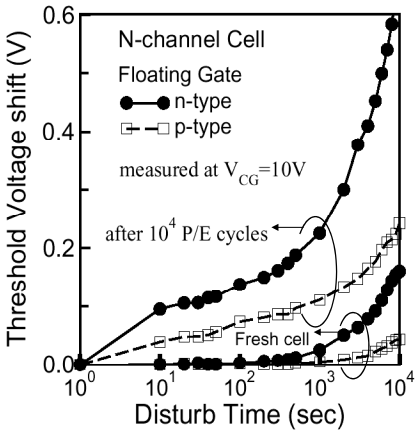

Fig. 6 The high oxide field gate-disturb characteristics for both n- and p-type floating-gate flash cells before and after 10^4 P/E cycles (N-channel cell).

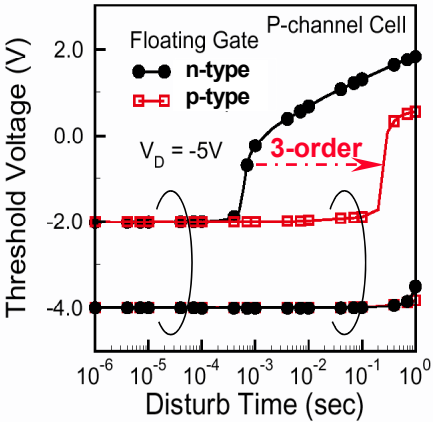

Fig. 9 Drain-disturb of p-channel cells under high oxide field. Note that drain-disturb has 3-order improvement by using p-type FG(square symbol).

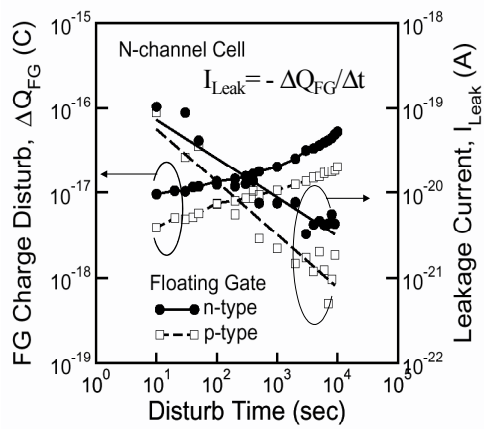

Fig. 7 Time evolution of the calculated SILC component due to trap-assisted tunneling at high oxide field (N-channel cell).

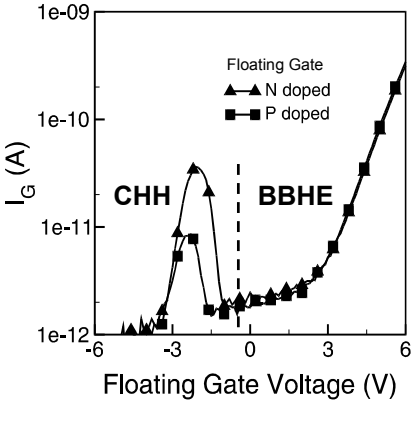

Fig. 10 The gate currents of p-channel flash cells with n- and p-type floating gate. The p-type FG cell has less gate current injection during CHH injection.