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New Three Dimensional High Density S-SGT Flash Memory Architecture using Self-Aligned Interconnection Fabricating Technology without Photo Lithography Process for Tera Bits and Beyond

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Abstract: New three dimensional S-SGT flash memory architecture can achieve the cell area of $3.88F^2$ per bit using 0.2um design rule. The new architecture is realized by stacking two select transistors and two memory cells in vertically on each pillar located in a two-dimensional array matrix. Each gate and each interconnection of this new architecture are fabricated by vertical self-aligned process and horizontal self-aligned process simultaneously using conformal deposited HTO and RIE without using photo lithography process. The new three dimensional S-SGT flash memory architecture is applicable to high-density nonvolatile memories as large as Tera-bits and beyond.(Keywords: Flash memory, S-SGT flash memory, Self-aligned interconnection fabricating technology.)

Introduction: Surrounding Gate Transisitor (SGT) was proposed in order to achieve future VLSI devices with high packing density [1], and an SGT DRAM cell was proposed [2]. In order to overcome the limitation of $4F^2$ per bit in conventional NAND Flash Memory cells [3] without using multi bit per memory cell technology, a Stacked–SGT (S-SGT) structured cell was proposed[4]. However, how to fabricate interconnections between each memory cells in order to make two dimensional memory array matrix using S-SGT structured cell was not presented.

In this paper, self-aligned interconnection fabricating technology is proposed, in order to realize new three dimensional high density S-SGT flash memory architecture. The new architecture is realized by stacking two select transistors and two memory cells in vertically on each pillar located in a two-dimensional array matrix. Each gate and each interconnection of this new architecture are fabricated by vertical self-aligned process and horizontal self-aligned process simultaneously using conformal deposited HTO and RIE without using photo lithography process. This new three dimensional S-SGT flash memory architecture can achieve the cell area of $3.88F^2$ per bit using 0.2um design rule. This paper describes the memory array architecture, fabrication process and operation principle of the new three dimensional high density S-SGT flash memory architecture.

Memory architecture: The new three dimensional high density S-SGT flash memory is structured by the array of S-SGT pillars. Fig.1 shows the architecture and the equivalent circuit of the new three dimensional high density S-SGT flash memory. In one pillar, source line, first select gate transistor (SG1), first flash memory cell(MC1), second flash memory cell(MC2), second select gate transistor(SG2) and bit line are stacked in series vertically [3]. The gates of SG1 are interconnected by the select-line 1 (SL1) along the row direction and separated along the column direction. The control gates of MC1 are interconnected by the word-line 1 (WL1) along the row direction and separated along the column direction. Similarly, MC2 and SG2 are inter-connected by word-line 2 (WL2) and select-line 2 (SL2) respectively.

Fabrication process: The new three dimensional high density S-SGT flash memory is fabricated using a 0.2um process. The concept of self-aligned interconnection fabricating technology is as follows. Fig.2 shows the top view of silicon pillar array after HTO conformal deposition, following poly-silicon deposition. The distance between silicon pillar along row direction d_{row} is designed enough narrower than two times the sum of the thickness of the poly-silicon and that of HTO. Fig.3 shows the self aligned interconnection fabricating sequence by using the cross sectional view of A-B-C in fig.2. As shown in the figure, HTO can bury the space between the pillar along the row direction which is designed narrower than twice as long as the deposited HTO thickness. On the other hand HTO cannot bury the space between silicon pillars along column direction which is designed wider than twice as long as HTO thickness. After CDE of poly-silicon followed by HTO RIE, the poly-silicon in the narrower space remains and that in the wider space is etched away. Using this concept, new three dimensional high density S-SGT flash memory architecture is formed as shown in fig.4. Firstly the silicon pillar is formed and gate oxidation is carried out followed by poly-silicon deposition. Then HTO conformal deposition is carried out. The bottom region between silicon pillars along the row direction is buried with HTO, because the space of this region is narrower than twice as long as HTO thickness. On the other hand the bottom region between the pillars along column direction is not buried with HTO, because the space of this region is wider than twice as long as HTO thickness. According to the concept shown in fig.3, HTO RIE (Step B), Poly-silicon RIE and HTO removing are carried out sequentially to form SL1 and select gate 1 (the gate of SG1). Simultaneously, the floating gate of MC1 and the floating gate of MC2 are formed. Repeating these process again the control gate of MC1 and the WL1 is formed simultaneously. Similarly, the control gate of MC2 and WL2 are formed simultaneously. And the gate of SG2 and SL2 are formed simultaneously. Through these fabrication process described, the high density S-SGT and the stacked interconnection lines are formed by vertical self-align process and by horizontal self-align process simultaneously without using photo lithography process.

Cell Operation: Fig.5 shows an equivalent circuit and operation voltage. In the erase operation, -25V is applied to all control gates, while keeping the bit line, source line and substrate grounded, and applying all select gates to +3V. Therefore, the threshold voltage (Vt) for all memory cells becomes negative. In the write operation, +25V is applied to the selected control gate, while keeping the bit line, source line and substrate grounded, and applying the unselected control gate and all select gates to +3V. Therefore, the threshold voltage (Vt) of the selected memory cell becomes positive. As a result, the S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler-Nordheim (F-N) tunneling electrons over the whole channel area of the memory cell, respectively, so called a bi-polarity F-N tunneling write/erase technology. In read operation, 0V is applied to the selected control gate, source line and substrate, and +3V is applied to the unselected control gates, the bit line, all select gates.

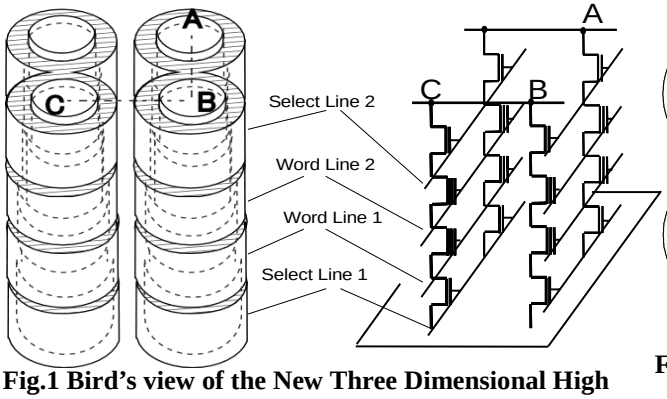

Fig.1 Bird's view of the New Three Dimensional High Density S-SGT Flash Memory and it's equivalent circuit.

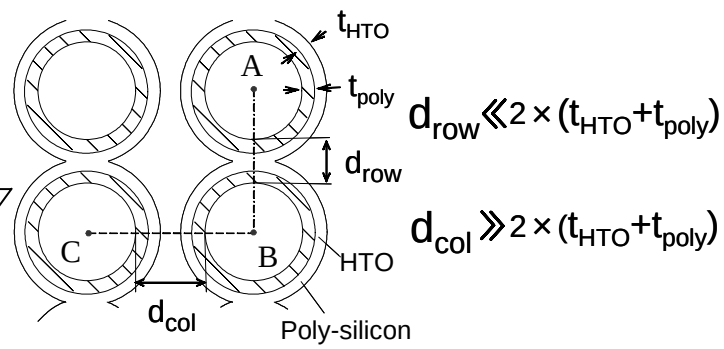

Fig.2 Top view of pillar array after HTO conformal deposition, following poly-silicon deposition.

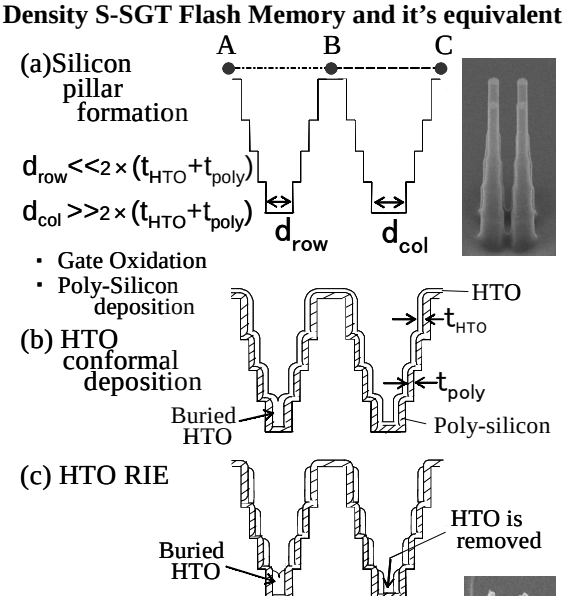

Fig.4 New Three Dimensional High Density S-SGT Flash Memory fabrication sequence.

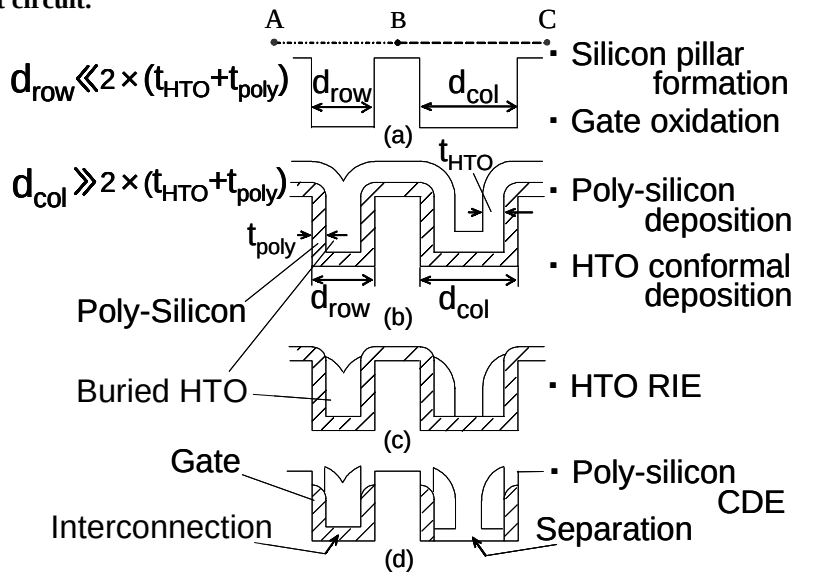

Fig.3 Self-Aligned Interconnection Fabricating sequence.

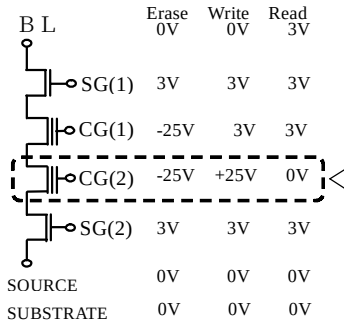

Fig.5 Equivalent circuit and operating voltages of the S-SGT Structured cell.

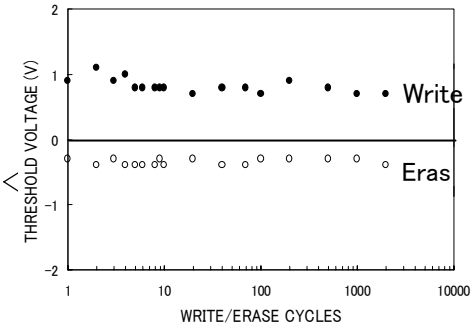

Fig.6 Endurance Characteristics of the S-SGT Structured cell.

The endurance characteristic of S-SGT structured Flash cell is shown in Fig.6. For S-SGT structured Flash cell with a bi-polarity write/erase operation method, excellent endurance characteristics are demonstrated. This endurance characteristic of S-SGT structured Flash cell is the most suitable for the Tera-bits Flash memories.

Conclusion: New three dimensional S-SGT flash memory architecture can achieve the cell area of $3.88F^2$ per bit using 0.2um design rule. Each gate and each interconnection of the S-SGT flash memory architecture are fabricated using vertical self-align process and horizontal self-align process simultaneously using conformal deposited HTO and RIE without using photo lithography process respectively. More over a highly reliable S-SGT structured Flash Memory has been successfully developed by using a bi-polarity F-N tunneling write/erase technology. The new three dimensional S-SGT flash memory architecture is applicable to high- density nonvolatile memories as large as Tera-bits Flash Memory and beyond.

Reference

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