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Key Technologies of First 'Chain' – 32Mbit Ferroelectric RAM

T.Ozaki, N.Nagel, Y.Kumura, J.Lian, A.Hilliger, T.Tsuchiya, R.Bruchhaus, H.Kanaya, H.Koyama, U.Wellhausen, O.Hidaka, S.Shuto, S.Gernhardt, Y. Shimojo, B.K.Moon, H.Itokawa,U.Egger, H.Zhuang, K.Tomioka, M.Fukushima, K.Yamakawa, D.Takashima, I.Kunishima, Y.Oowaki, and G.Beitel

Semiconductor Company, Toshiba Corporation, Infineon Technologies Japan K.K.

FDA. Yokohama Complex #410-1F, 8 Shinsugita-cho, Isogo-ku, Yokohama, 235-8522 Japan

+81-45-770-3917; E-mail: ozaki@amc.toshiba.co.jp

Abstract

A 32Mbit ferroelectric RAM (FeRAM) based on a 0.2μm DRAM technology is successfully fabricated employing a capacitor on plug structure with a highly reliable Pt/SRO/PZT/SRO/Pt capacitor on a double Ir oxidation barrier and a CoSi Si diffusion barrier. A chip size of 96mm^2 is achieved using a 'Chain' cell structure.

Key Technologies of our 32Mbit FeRAM

Figure 1 shows key features of our chip. The 02μm generation DRAM technology is employed for the FEOL (front end of line). Co-salicide is adapted on poly Si plug to avoid Si diffusion into the barrier. A so-called double Ir barrier (1), with additional RTA steps to stuff the grain boundaries, is used as oxidation barrier. A 0.6um square Pt/SRO/PZT/SRO/Pt stacked capacitor is applied to get high reliable operation (2-4). A steep taper of top electrode (TE), ferroelectric layer (FE), and bottom electrode (BE) is obtained using high temperature (HT) (250C - 350C) RIE (5). To avoid degradation of the capacitor during metallization a dual damascene process with Nb liner, which assists the Al – reflow process, is used (6). To obtain high cell efficiency, the 'Chain' cell structure (7) is employed. A SEM picture of 32Mbit ferroelectric RAM is shown in fig.2. And a chip image and specifications are listed in fig.3. Due to the high cell efficiency of 'Chain' architecture, 96mm^2 chip area is achieved.

Fabrication results

A W – plug is formed over DRAM like transistors. After covering the W - plug with LP-SiN / LP-TEOS, CP (contact for capacitor plug) holes with additional round etching are formed. The CP holes are filled by N+ poly Si, using a CMP technique. The CoSi layer is formed on top of the poly plug by a salicide technique. Ti/Ir oxygen barrier and Pt/SRO bottom electrode are formed on the plug. Then PZT and SRO/Pt top electrode are deposited. 75 degree TE/FE and BE shape are achieved by HT RIE process. To realize the 'Chain' cell structure (double TE on one BE), we employed a 2 step RIE process for capacitor formation. Finally, 3 level dual damascene process is employed for less damage from the BEOL (back end of line) to the capacitor.

Poly Si plug with CoSi Si diffusion barrier

Si from the poly plug can easily diffuse into the Ir barrier during thermal heating forming the capacitor. To avoid this Si diffusion, a CoSi layer on top of poly plug is adapted. The Co salicide process formation is easily introduced to the plug process, because the process is completely the same as for usual logic processes. If there is a dip at the center of the poly plug a defect in the CoSi layer appears. By rounding the void is formed in the upper part of the CP contact and the CoSi layer remains intact. Figure 4 shows TEM result of the CP region. No indication of Si diffusion can be seen. A Co salicide layer is smoothly formed on N+ poly Si plug in a self-aligned manner. Due to cleaning before the Co sputtering process, a slight step appears between TEOS and the top of the CoSi layer. However, no bad effect is identified from this very small plug step. Element analysis results are shown in fig.5. No Si diffusion is seen, and Co, Ti and Ir are also stable. Furthermore, no indication of plug oxydation is seen from oxygen image. In addition the etching shape of TE/FE can be seen in the TEM. FE was completely etched and no fence appears using a HT (350C) RIE process.

Evaluation results

Cumulative probability of CP contact resistance in the case of double Ir barrier and 'with IrO_2' is shown in Fig. 5. For both cases the resistance increase with the temperature. This behavior is supposed to be caused by slight Si diffusion and oxidation. For the 'with IrO_2' case, barrier performance for oxidation is higher than for the double Ir case. Therefore 'with IrO_2' case shows lower 'CP' resistance. However, we could get resistance less than 2.5kΩ after full process. Even in double Ir case, resistance value still stays low enough. Hysteresis shape of a 0.6μmx0.6um TE size test structure and the TE size dependence of switching charge are shown in fig.6. Good hysteresis shape and Qsw of 20uC/cm^2 for target size are achieved. To increase 1T1C operation margin, we should increase the switching charge more. A functional result is shown in figure 7, our chip works with 50ns access speed in 3.0V supply voltage.

Conclusion

A 96mm^2 32Mbit FeRAM chip with 'Chain' cell structure is successfully fabricated using a Co salicide Si diffusion barrier, a HT RIE process for the capacitor and the double Ir /Pt /SRO /PZT /SRO/Pt stacked capacitor. In addition, we could achieve CP contacts with resistance <2.5kΩ and Qsw of 20uC/cm^2 in target TE size. As a result, the functional chip can be realized with our novel technologies.

References

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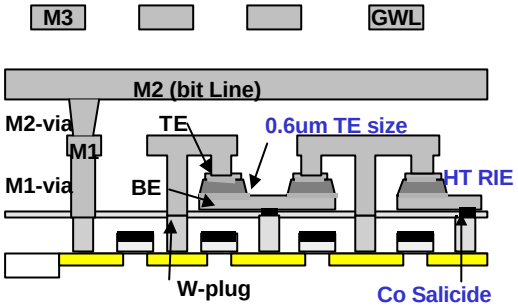


Fig.1 Keys technology of our FeRAM

COP structure with CoSi Si diffusion barrier and HT RIE process are key of our FeRAM with 'Chain' cell structure

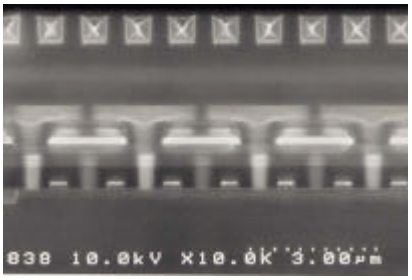
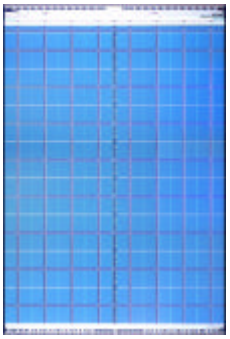


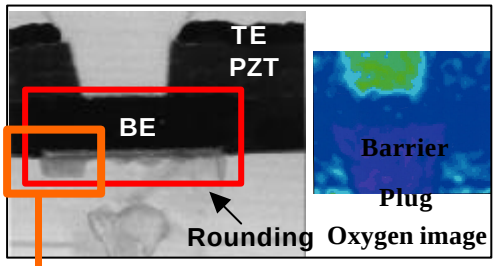
Fig.2 SEM picture memory cell

Cross section corresponding to fig.1



Organization	*32Mb = 2Mb x 16*
Capacitor size	*0.36um2 (0.6x0.6)*
Chip size	*96mm²*
Cell size (ave.)	*1.8753um²*
Chain length	*8 cell / chain*
Cell Efficiency	*65.6%*
Power supply	*3.0V / 2.5V*
Access / Cycle	*50ns / 75ms*
Active / Standby	*30mA / 3uA*

Fig.3 32M chip image *Specifications are listed above*



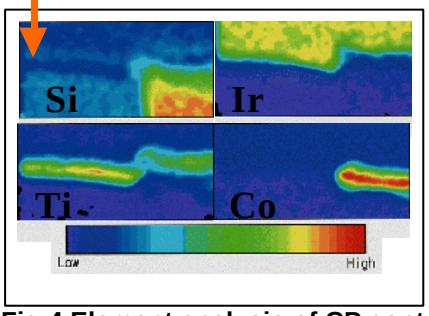


Fig.4 Element analysis of CP contact

In 600C process Si, Ir, Ti, Co layers are stable and there is no indication of oxidation on Si plug

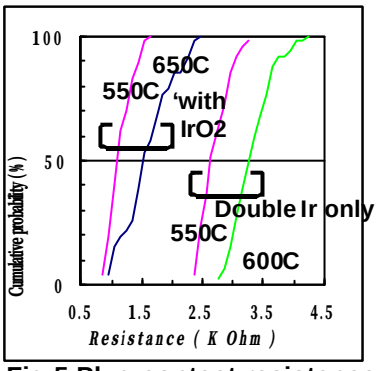


Fig.5 Plug contact resistance

Double Ir can be applied up to 600C process and IrO2 on double Ir has effect to avoid oxidation of Si plug even in 650C process.

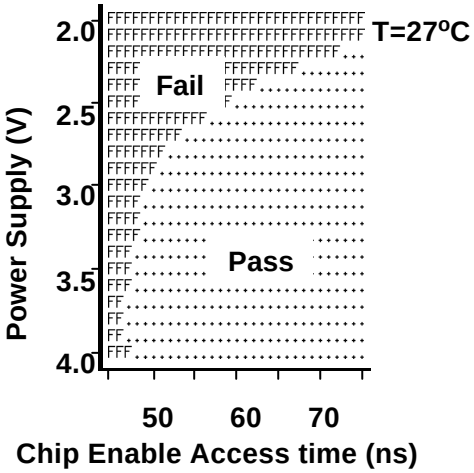


Fig.7 Shmoo plot of our chip

50ns Access time is achieved in 3.0V supply voltage

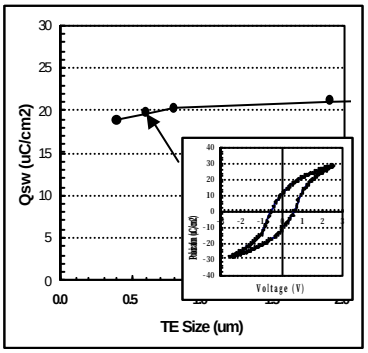


Fig.6 TE size dependence

20uC/cm2 of Qsw is achieved in our FeRAM process.