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High Performance Pt/ $SrBi_2Ta_2O_9$/ HfO_2/ Si Structure for 1T Ferroelectric Random Access Memory

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1. Introduction

Metal-ferroelectric-insulator-semiconductor (MFIS) structure has attracted considerable attention as a promising candidate for high-density and high-speed field effect transistor (FET)-type memories [1]. An additional insulating layer is needed because of the possible reaction and interdiffusion between the ferroelectric film and the silicon substrate [2]. Therefore, finding a suitable insulating layer with sufficient thermal stability becomes the key issue in pursuing the NDRO low-voltage and high-density FeRAMs [3].

In this work, we employ an HfO_2 thin film as the insulating layer for fabricating MFIS capacitors. HfO_2 -based high-κ dielectric is extremely attractive because of its high thermal stability, high interface quality on silicon, and relatively high κ value [4]. It is found that the memory window of such a stack structure can be as large as 1.08V at a very low operation bias of 3.5V. More importantly, it exhibits excellent endurance against switching degradation up to 10^9 cycles.

2. Experimental

The MFIS capacitors were fabricated on 6-inch (100) p-type silicon wafers. The 8nm-thick HfO_2 film was deposited by atomic vapor deposition on an AIXTRON Tricent® system at 400 ^oC in oxygen ambient, and then annealed at 1000 ^oC for 30 sec in nitrogen atmosphere. Subsequently, the $SrBi_2Ta_2O_9$ film was deposited by MOD technique subjected to a baking sequence; the conditions of which were 120 ^oC, 250 ^oC, and 400 ^oC for 10 min in air. After the target film thickness of about 390 nm was achieved, the film was crystallized at 750°C for 3 min by RTA in O_2 atmosphere. Finally, Pt was deposited to serve as the top electrode by electron beam evaporation.

3. Results and Discussion

The XRD pattern of the $SrBi_2Ta_2O_9$ thin film is illustrated in Fig. 1(a). Sharp peaks indicative of well -crystallized perovskite phase imply that HfO_2 film can serve as a seed layer for SBT crystallization. The resultant SBT film is polycrystalline with the predominant orientations of (115) and (200), which are favored in term of polarization. The crystalline microstructure of the SBT film is also analyzed by AFM. As shown in the inset of Fig. 1(a), the film depicts surface morphology with uniformly distributed and considerably large grains (~80nm). The SIMS depth profile in Fig.1(b) displays extremely well resistance of HfO_2 against inter-diffusion between the SBT film and substrate. These distinctive features, we believe, are the keys to the low voltage operation.

Figure 2 shows the capacitance-voltage (C-V) curves of the Pt/$SrBi_2Ta_2O_9$/HfO_2/Si structure. Window of 1.08V is clearly demonstrated in a back-and-forth voltage sweep between -3.5V and 3.5V. The estimated ratio of the memory window to the applied voltage, as shown in the inset of Fig. 2, is 26.4%. Such excellent performance is ascribed not only to the well-crystallized perovskite structure of the SBT film but also large capacitance and high quality of the underneath HfO_2 thin film. The EOT of the accompanying Pt/HfO_2/Si test structure is only about 2.8 nm. Based on the voltage divider principle for in-series capacitors, the applied voltage will mostly drop across the SBT film, which in turn leads to a well-saturated polarization behavior for the ferroelectric SBT film. Moreover, only negligible hysteresis arising from traps in the bulk has appeared in the back-and-forth C-V sweeping. This characteristic is extremely crucial because this type of hystereses always act in opposite direction with that in polarization.

Several bipolar pulse trains with 3.0V, 3.5V, and 4.0V in amplitude and a pulse width of 2 microseconds were employed for testing the switching characteristics of the Pt/SBT/HfO_2/Si structure. The endurance results are shown in Fig. 3(a). After switching over 10^9 times, the degradation of the memory window is found to be only about 9 to 15% under different stress biases. In the inset of Fig. 3(a), it is demonstrated that the degradation is inclined to occur in on-state (V_-). This may result from

the electron trapping or pinning of domain during the stress period. To further examine the degradation after stress, the leakage current characteristics of the Pt/SBT/HfO_2/Si structure before and after cycling are shown in Fig. 3(b). It can be seen that up to 10^9 switching cycles cause almost no leakage current degradation below 4V gate bias.

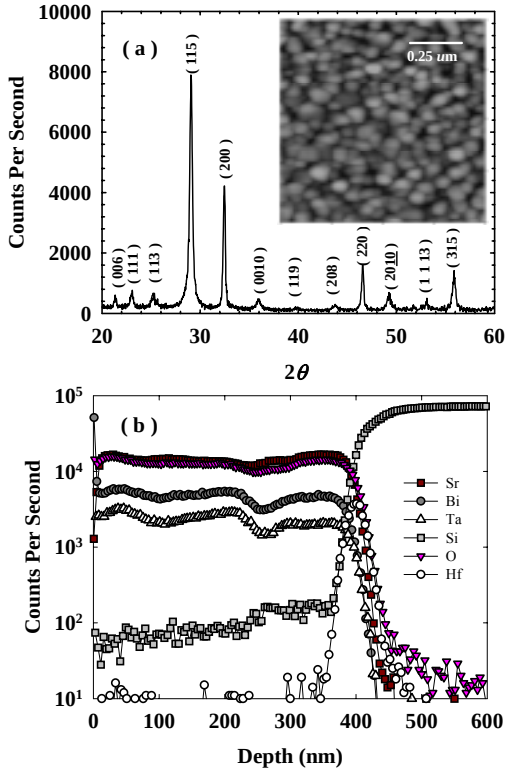

Fig. 1. (a) XRD pattern and (b) SIMS depth profile of SBT/HfO_2/Si structure. The inset shows the morphology of the SBT surface. The area of the picture is 1 um^2.

4. Conclusions

In summary, we have demonstrated the feasibility of fabricating MFIS capacitors with 390nm-thick $SrBi_2Ta_2O_9$ ferroelectric film and 8nm-thick HfO_2 dielectric film on silicon substrate. It is shown that the Pt/$SrBi_2Ta_2O_9$/HfO_2/Si (MFIS) structure can provide a memory window as large as 1.08V at an operation voltage of 3.5V. In addition, it also exhibits excellent switching characteristics with only 9 to 15% degradation in memory window after 10^9 switching cycles with different pulse train voltages. These results indicate that HfO_2 is extremely suitable for the low-voltage and high-density NDRO FeMFET applications.

Acknowledgment

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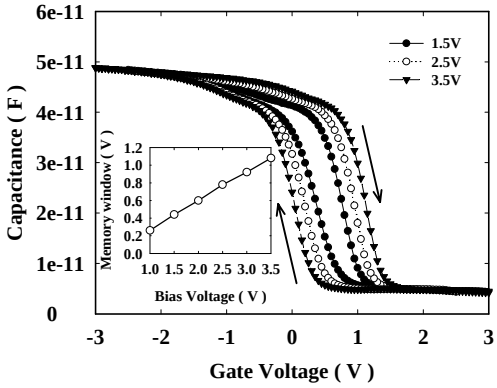

Fig. 2. High frequency capacitance-voltage characteristics of Pt/SBT/HfO_2/Si structure with different sweeping voltages. The memory window is 1.08V at a sweeping voltage of 3.5V. The inset shows that the memory window is a function of sweep voltage. The slope is about 26.4%.

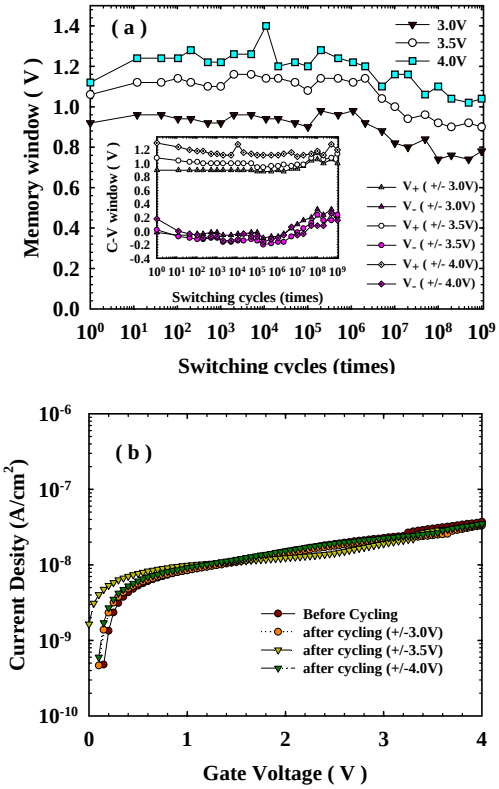

Fig. 3. (a) Memory window as a function of switching cycles. The inset shows the voltage shift of the MFIS capacitor under different pulse train voltage. (b) Current-voltage characteristics before/after 10^9 switching cycle for Pt/SBT/HfO_2/Si structure.

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