Improvement in Read Endurance of Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode

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1. Introduction
Ferroelectric gate field-effect transistor memory (F-FET) has been widely investigated because of its novel features of non-destructive reading, high operation speed and high packing density. However, F-FET has not been commercialized due to some technological difficulties such as short retention time, high operation voltage and unstable performance. As an attempt to put F-FET into practical, Shimada et al. and Horita et al. proposed a new operation of F-FET with an intermediate electrode between the ferroelectric film and the MOSFET [1]. The memory cell consists of a ferroelectric capacitor Cf with typical ferroelectric film and the MOSFET [1]. The memory cell consists of a ferroelectric capacitor Cf with typical polarization – electric field (P-E) hysteresis loop as in Fig. 1, connected to the gate of a MOSFET, as illustrated in Fig. 2. For data writing, a writing voltage Vw is applied only to Cf. If the Cf with positive remanent polarization Pr is positively biased, the ferroelectric capacitance Cfh is large. If the Cf with negative remanent polarization Pf is positively biased, the ferroelectric capacitance Cfl is small. Therefore, when a positive reading voltage VR is applied to both the Cf and MOSFET, corresponding to the polarization states of Cf, the intermediate voltage VI is different, leading to a different drain current ID. By detecting the ID, the memory state is decoded.

Fig. 1. A typical P – E hysteresis loop of Cf

Fig. 2. Experimental circuit and conditions.

However, the new F-FET encounters a decrease of VI during a consecutive reading which may lead to a short read endurance. The origin of the decrease of VI was found to be a small leakage current through the writing MOSFET (W-FET) which is connected between the intermediate electrode and the source of the reading MOSFET (R-FET). The W-FET is used as a switch for integration. This configuration is termed source-connected configuration (SCC). To enhance the read endurance, we change one end of the W-FET from the source to the drain of the R-FET. This arrangement is termed drain-connected configuration (DCC). In this conference, we show that the read endurance is much improved with DCC, then the results are analyzed and theoretically verified.

2. Theoretical consideration
The VI is decreased due to electrons flowing into the intermediate electrode through the W-FET from the source. So, more reading cycles make VI decreased and Vf (the voltage on Cf) increased because Vf = VI + Vr = constant. This means that the Cf dependent on Vf, is varied with reading cycle, in particular, for the Pr state. On the other hand, when the applied Vw changes from high to zero at the first reading pulse, the VI falls not to zero as normally predicted but to a voltage Vp [1], in which Vr = -Vp≠0. Also, from the second reading pulse, the VI is added by the Vp regardless of Vr. The Vp originates from the polarization domains which do not return to their virgin remanent polarization states once switched by Vr. Consequently, positive charges are induced in the intermediate electrode and produces Vp. The non-returning domains may be produced when the Vf during a reading is over the maximum Vf during the adjacent previous reading. Also, as mentioned above, since the VI is increased with the reading cycle, the Vp is possibly increased with it. Defining ∆VI as the increment of VI, the increment of Vp, ∆VP, can be expressed by ∆VP=k∆VfΔCf(Cf+C0)-1 (1), where ΔCf = Cf(Vf) – Cf(Vf=0), C0 is the input capacitance of R-FET and k is the non-returning domain ratio. Also, kΔVfΔCf is the non-returning domain charge added to Qf at the intermediate electrode.

We calculate the time dependent VI(t) for the DCC where t is a time from the start of measurement. Because a unipolar reading square pulse voltage VR is a superposition of a bipolar square pulse with a square wave function S(t)=±1 as AC part and a DC offset. The VI has an AC part, VIAC, due to AC part of VR and a transient part, VI(t), with a time constant τ of the circuit. The VI consists of three parts. The first one is generated by the DC offset of VR, which is
can be obtained by setting \( V_D = 0 \) in (2).

Fig. 3 shows output voltage \( V_0 \) as a function of reading cycles for the SCC. The C \( f \) was determined from a corresponding P-V hysteresis loop. For the SCC, the difference in behavior of \( \Delta V_0 \) between the \( P_r \) and \( P_p \) states can be explained as follows. There are three factors contributing to \( \Delta V_0 \): the non-returning domain charge as origin of the \( \Delta V_0 \) in the simulation, the \( C_t \) and the time constant \( \tau = \frac{C_t + C_0}{R} \). The larger \( \Delta V_0 \) in the \( P_r \) state than in the \( P_p \) state are attributed to 1) larger \( \tau \) and 2) non-zero \( \Delta V_p \) in the former state. The larger \( \tau \) is due to \( C_b \) larger than \( C_0 \) and \( \Delta V_p = 0 \) in the \( P_p \) state is due to \( C_t = \text{const.} \) and \( \Delta C_t = 0 \). These discussions are also acceptable for the DCC.

3. Experimental

The experimental circuit used to investigate the consecutive read endurance is shown in Fig. 2. The \( C_t \) was a 200-nm-thick epitaxial grown PZT film on a Si substrate. Details of preparation of the film can be found in [2]. The R-FET is a self-made MOSFET. To simulate the W-FET in OFF state, a twin diode formed by connecting two identical diodes back to back was used for both the SCC and DCC (the dashed line in Fig. 2). The leakage current of the twin diode was about 1 pA at 1V.

4. Experimental results and discussions

Fig. 3 shows output voltage \( \Delta V_0 = V_0 - V_{DR} \) as a function of reading cycle for the SCC. For the \( P_r \) state, the \( \Delta V_0 \) starts decreasing with reading cycles of more than \( 3 \times 10^7 \). For the \( P_p \) state, the \( \Delta V_0 \) is even decreased faster and finally reached to a saturation of nearly zero. Fig. 4 shows \( \Delta V_0 \) as a function of reading cycles for the DCC. Contrary to Fig. 3, for the \( P_r \) state, \( \Delta V_0 \) is almost constant with the reading cycle up to \( 6 \times 10^7 \). For the \( P_p \) state, the \( \Delta V_0 \) is slightly decreased or unchanged.

To carry out the simulation, the differential capacitance \( C_t \) is to be determined from a corresponding P-V hysteresis loop. For the SCC and DCC, the simulated results are plotted together with the experimental data for a comparison in Figs. 3 and 4 where the bold lines are for \( k = 0.8 \) and the fine lines are for \( k = 0 \). It can be seen that the simulation results are in good agreements with the experimental data for \( k = 0.8 \), which means that our model is physically acceptable. Also, we can recognize that the non-returning domains contribute to \( \Delta V_p \). For the SCC, the difference in behavior of \( \Delta V_p \) between the \( P_r \) and \( P_p \) states can be explained as follows. There are three factors contributing to \( \Delta V_p \): the non-returning domain charge as origin of the \( \Delta V_p \) in the simulation, the \( C_t \) and the time constant \( \tau = \frac{C_t + C_0}{R} \). The larger \( \Delta V_p \) in the \( P_r \) state than in the \( P_p \) state are attributed to 1) \( C_0 \) larger than \( C_0 \) and 2) larger \( \Delta V_p \) for the former state. This larger \( \Delta V_p \) is due to larger \( C_b \) which has many ferroelectric domains subject to switching. The slower decrease of \( \Delta V_p \) in the \( P_r \) state than in the \( P_p \) state are attributed to 1) larger \( \tau \) and 2) non-zero \( \Delta V_p \) in the former state. The larger \( \tau \) is due to \( C_b \) larger than \( C_0 \) and \( \Delta V_p = 0 \) in the \( P_p \) state is due to \( C_t = \text{const.} \) and \( \Delta C_t = 0 \). These discussions are also acceptable for the DCC.

References