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Improvement in Read Endurance of Ferroelectric Gate Field-Effect Transistor Memory with an Intermediate Electrode

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1. Introduction

Ferroelectric gate field-effect transistor memory (F-FET) has been widely investigated because of its novel features of non-destructive reading, high operation speed and high packing density. However, F-FET has not been commercialized due to some technological difficulties such as short retention time, high operation voltage and unstable performance. As an attempt to put F-FET into practical, Shimada et al. and Horita et al. proposed a new operation of F-FET with an intermediate electrode between the ferroelectric film and the MOSFET [1]. The memory cell consists of a ferroelectric capacitor C_f with typical polarization – electric field (P-E) hysteresis loop as in Fig. 1, connected to the gate of a MOSFET, as illustrated in Fig. 2. For data writing, a writing voltage V_W is applied only to C_f. If the C_f with positive remanent polarization P_r^+ is positively biased, the ferroelectric capacitance C_{fl} is small. If the C_f with negative remanent polarization P_r^- is positively biased, the ferroelectric capacitance C_{fh} is large. Therefore, when a positive reading voltage V_R is applied to both the C_f and MOSFET, corresponding to the polarization states of C_f, the intermediate voltage V_I is different, leading to a different drain current I_D. By detecting the I_D, the memory state is decoded.
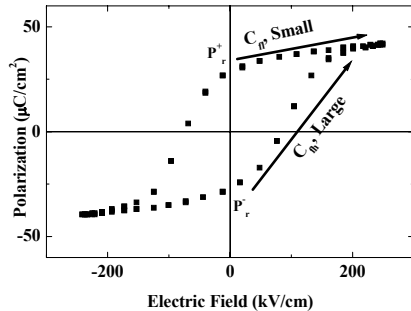

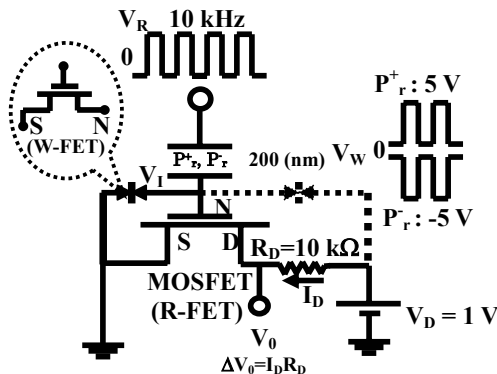**Fig. 1.** A typical P − E hysteresis loop of C_f

Fig. 2. Experimental circuit and conditions.

However, the new F-FET encounters a decrease of V_I during a consecutive reading which may lead to a short read endurance. The origin of the decrease of V_I was found to be a small leakage current through the writing MOSFET (W-FET) which is connected between the intermediate electrode and the source of the reading MOSFET (R-FET). The W-FET is used as a switch for integration. This configuration is termed source-connected configuration (SCC). To enhance the read endurance, we change one end of the W-FET from the source to the drain of the R-FET. This arrangement is termed drain-connected configuration (DCC). In this conference, we show that the read endurance is much improved with DCC, then the results are analyzed and theoretically verified.

2. Theoretical consideration

The V_I is decreased due to electrons flowing into the intermediate electrode through the W-FET from the source. So, more reading cycles make V_I decreased and V_f (the voltage on C_f) increased because $V_R = V_I + V_f = $ constant. This means that the C_f dependent on V_f, is varied with reading cycle, in particular, for the P_r^- state. On the other hand, when the applied V_R changes from high to zero at the first reading pulse, the V_I falls not to zero as normally predicted but to a voltage V_p [1], in which $V_f = -V_p \neq 0$. Also, from the second reading pulse, the V_I is added by the V_p regardless of V_R. The V_p originates from the polarization domains which do not return to their virgin remanent polarization states once switched by V_R. Consequently, positive charges are induced in the intermediate electrode and produces V_p. The non-returning domains may be produced when the V_f during a reading is over the maximum V_f during the adjacent previous reading. Also, as mentioned above, since the V_f is increased with the reading cycle, the V_p is possibly increased with it. Defining ΔV_f as the increment of V_f, the increment of V_p, ΔV_p, can be expressed by $\Delta V_p = k \Delta V_f \Delta C_f (C_f + C_0)^{-1}$ (1), where $\Delta C_f = C_f(V_f) - C_f(V_f=0)$, C_0 is the input capacitance of R-FET and k is the non-returning domain ratio. Also, $k \Delta V_f \Delta C_f$ is the non-returning domain charge added to Q_I at the intermediate electrode.

We calculate the time dependent $V_I(t)$ for the DCC where t is a time from the start of measurement. Because a unipolar reading square pulse voltage V_R is a superposition of a bipolar square pulse with a square wave function $S(t)=\pm 1$ as AC part and a DC offset. The V_I has an AC part, V_{IAC}, due to AC part of V_R and a transient term, V_{IT}, with a time constant τ of the circuit. The V_{IT} consists of three parts. The first one is generated by the DC offset of V_R, which is

decreased exponentially with t/τ. The second one is V_p which is also decreased exponentially with t/τ and the third one is from the V_D bias which increases with $[1-\exp(-t/\tau)]$. For a linear analysis, the whole range up to the total reading cycle is divided into M regions with linear systems. Within the ith region with N_i reading cycles, the intermediate voltage $V_{Ii}(t)$ is calculated as the following equation

$$V_{Ii}(t) = V_{IAC} + V_{IT} = 0.5\left(V_{I0i} - V_{p(i-1)}\right)S(t) + V_D + \quad (2)$$

$$+ \left[0.5\left(V_{I0i} - V_{p(i-1)}\right) + V_{p(i-1)} - V_D\right]\exp[-(t - \sum_{s=1}^{i-1} N_s T)\tau_i^{-1}].$$

In (2), V_{I0i} is the V_I at the first reading cycle of the ith region. Also, τ_i is the time constant given by $\tau_i=(C_{fi}+C_0)R$ and C_{fi} is a mean ferroelectric capacitance between $C_f(V_R =$ high) and $C_f(V_R=0)$ at the first reading cycle of the ith region. Furthermore, $V_{p(i-1)}$ is a sum of V_I at the end of the $(i-1)^{th}$ region with $S(t)=-1$ and ΔV_p due to ΔV_f generated in $(i-1)^{th}$ region according to (1). The calculation for the SCC can be obtained by setting $V_D = 0$ in (2).

3. Experimental

The experimental circuit used to investigate the consecutive read endurance is shown in Fig. 2. The C_f was a 200-nm-thick epitaxial grown PZT film on a Si substrate. Details of preparation of the film can be found in [2]. The R-FET is a self-made MOSFET. To simulate the W-FET in OFF state, a twin diode formed by connecting two identical diodes back to back was used for both the SCC and DCC (the dashed line in Fig. 2). The leakage current of the twin diode was about 1 pA at 1V.

4. Experimental results and discussions

Fig. 3 shows output voltage $\Delta V_0=I_D R_D$ as a function of reading cycle for the SCC. For the P_r^- state, the ΔV_0 starts decreasing with reading cycles of more than 3.0×10^7. For the P_r^+ state, the ΔV_0 is even decreased faster and finally reached to a saturation of nearly zero. Fig. 4 shows ΔV_0 as a function of reading cycles for the DCC. Contrary to Fig. 3, for the P_r^- state, ΔV_0 is almost constant with the reading cycle up to 6×10^7. For the P_r^+ state, the ΔV_0 is slightly decreased or unchanged.

To carry out the simulation, the differential capacitance C_f is to be determined from a corresponding P-V hysteresis loop. For the SCC and DCC, the simulated results are plotted together with the experimental data for a comparison in Figs. 3 and 4 where the bold lines are for k = 0.8 and the fine lines are for k = 0. It can be seen that the simulation results are in good agreements with the experimental data for k=0.8, which means that our model is physically acceptable. Also, we can recognize that the non-returning domains contribute to ΔV_0. For the SCC, the difference in behavior of ΔV_0 between the P_r^- and P_r^+ states can be explained as follows. There are three factors contributing to ΔV_0: the non-returning domain charge as origin of the ΔV_p in the simulation, the C_f and the time constant $\tau=(C_f+C_0)R$. The larger ΔV_0 in the P_r^- state than in the P_r^+ state are attributed to 1) C_{fh} larger than C_{fl} and 2) larger ΔV_p for the former state. This larger ΔV_p is due to

larger C_{fh} which has many ferroelectric domains subject to switching. The slower decrease of ΔV_0 in the P_r^- state than in the P_r^+ state are attributed to 1) larger τ and 2) non-zero ΔV_p in the former state. The larger τ is due to C_{fh} larger than C_{fl}, and $\Delta V_p=0$ in the P_r^+ state is due to $C_f \approx$ const. and $\Delta C_f = 0$. These discussions are also acceptable for the DCC.
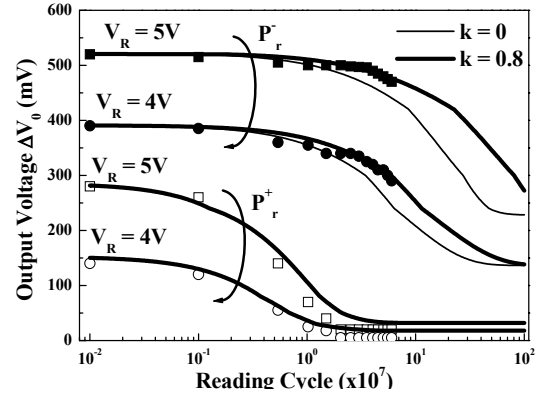

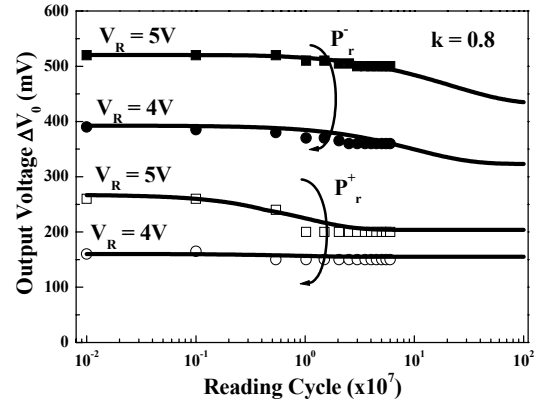**Fig. 3.** Dependences of ΔV_0 on reading cycle for SCC.

Fig. 4. Dependences of ΔV_0 on reading cycle for DCC.

According to the simulation, for both cases, the ΔV_0 finally reaches a saturation value corresponding to a saturation value of V_I, $V_I(t\to\infty)=C_{f\infty}V_R[2(C_{f\infty}+C_0)]+V_D$, where the $C_{f\infty}$ is C_f at a saturated V_f. Because the $C_{f\infty}$ for the P_r^+ state is different from the one for the P_r^- state, $V_I(t\to\infty)$ is also different from each other. Therefore, ΔV_0 saturates at much higher value for the DCC than for the SCC.

5. Conclusions

Physical phenomena and mechanisms of a new F-FET memory operation have been investigated. It is experimentally and theoretically verified that the DCC is a good solution to achieve high read endurance.

References

[1] S. Horita and T.D.Khoa, Jpn. Appl. Phys. **42,** 2003, pp. L365-L368.

[2] S. Horii, S. Yokoyama, T. Kuniya, S. Horita, Jpn. J. Appl. Phys., 39, 2000, pp. 2114-2118.