Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 652-653

P10-7

A Novel Sensing Circuit for High Speed Synchronous MRAM

Hyejin Kim, Seungyeon Lee, Seungjun Lee, Hyungsoon Shin and Daejung Kim[1]

Ewha Womans University, Dept. of Information Electronics Engineering
Daehyun-Dong, Seodaemun-Gu, Seoul 120-750, Korea
Tel : +82-2-3277-2804 E-mail: slee@ewha.ac.kr
[1]Kookmin University, Dept. of Electronics Enginerring
861-1 Chongnung-dong, Songbuk-gu, Seoul, 136-702, Korea

1. Introduction

Magneto-resistive random access memory (MRAM) has many advantages as future non-volatile memory, so MRAM architectures has been studied for a long time [1][2]. To guarantee robust MRAM operation, the most critical issue is magneto-resistance (MR) degradation. MR ratio is reduced considerably as the voltage across the magnetic tunnel junctions (MTJ) reaches the critical value. Several prototypes of MRAM reported so far take current-sensing type of sensing scheme to cope with MR degradation [4][5][6]. Due to the large size of current-sensing sense amplifiers, the previous architectures can't follow practical DRAM or SRAM architectures that allow page-mode operation for high-speed synchronous read-out. In this paper, we propose a noble MRAM sensing circuit which is small enough to fit into 1~2 column pitches like those used in DRAMs while providing stable operations.

2. Architecture

MR ratio is dependent upon the change of voltage applied to the MTJ. It changes little with a small voltage bias, whereas it decreases significantly at higher bias. It is reduced to half when the voltage reaches the critical value such that it cannot function as a storage element. Therefore, it is critical to control the voltage applied to the MTJ not to reach the critical value which is in the range of 0.6V~1.0V. The proposed sensing scheme uses a conventional cross-coupled latch type sense amplifier while keeping the bias voltage across the MTJ being lower than the critical value.

Architecture and Operation

Fig 1. shows proposed sensing scheme. Our scheme is based on 2MTJ-2T cell structures for larger sensing margin and reliable operation at high speed. The sense amplifier has the same structures as that of DRAM except two current sources and one additional transistor for I_{bit} current loop. The bias voltage across MTJs remains below the critical voltage by limiting the gate voltage of pass transistors (BCK_SEL) between bit lines and the sense amplifier.

Current source at each bit-line provides the same amount of current to the both MTJs and produce voltages difference due to the different resistances of the MTJs. The voltage difference of MTJs is slightly amplified while passing through the block select transistors. Finally, it is fully developed when the sense amplifier is activated. At this moment, high voltage at SA,/SA node can be applied to the voltage across MTJs through the BCK_SEL transistors and can produce degradation of MR ratio. If the voltage of BCK_SEL is kept to half V_{dd} or below that, the voltage at the source node of BCK_SEL transistor cannot exceed '$1/2V_{dd} - V_{TN}$'. Therefore, without any complicated sensing scheme, the voltage across MTJs can be controlled below the critical value.

Fig 2. shows simulated waveform of the sensing operation. Initially BIT, /BIT are set to Gnd. When a word-line is selected and current sources become active, the bit line pair shows the voltage difference of about 100mV due to the difference of MTJ resistances. Then, the sense amp is enabled and the data is fully developed to V_{core} (=2.5V) and Gnd. The voltage between MTJ, measured as 'BIT – pass TR' in the figure, remains less than 400mV during the whole operation.

In program mode, the bit line pair form a current loop so that WE is set to the high state[3]. The data at the write driver decides the direction of the current through the bit line. At the same time, a digit line driver is enabled and I_{digit} current flows through the digit line. Therefore I_{bit} and I_{digit} make magnetic field that can reverse the polarization of the soft layer of MTJ. The low gate voltage on BLK_SEL transistor shows high resistance during write operation. This is not desirable because the write operation requires large current of about 1mA on the bit line. So, voltage control circuit is added to switch the gate voltage to full V_{dd} in program mode.

To verify out sensing circuit, we designed 256-bit synchronous MRAM using 0.35μm technology. The resistance of the MTJs are 20k and 29.5k (the MR ratio is 30%). Fig 3. shows the array schematic of the full chip. The cell array consists of 8 word line and 32 bit line pair, so that the total size is 256 bits. We adopt shared sense amplifier structure. Our sense amplifier has small enough that the layout can fit into 4-cell pitches. Once a word-line is selected, 32 sense amplifiers are activated at the same time and 32 bit data are latched for high-speed read-out afterwards.

Simluation Result

Fig 4. shows a full chip simulation result at 100MHz burst mode operation(CL=2, BL=4). The simulation shows one burst-mode write and one burst-mode read. The data (1,0,1,0) is written to the cell first, and read out in the next cycle. Fig 5. shows a full chip layout. Even though the current implementation contains only 256bit cells, it can be readily extended to ~Mbit MRAM once TMR uniformity is guaranteed.

3.Conclusion

By means of limiting control signal voltage, we can safely adopt the sense amplifier of DRAM to an MRAM. The size of this sense amplifier is small enough to fit into the 4-cell pitch, so the page mode can be possible in MRAMs. 256bit synchronous MRAM is designed using 0.35μm technology, and it shows reliable operation at 100MHz.

References

[1] Tzu-Ning Fang and Jian-Gang Zhu, *IEEE transactions on magnetics* (2001)

[2] Geral B. Granley and Allan T. Hurst, *1996 Int'l Nonvolatile Memory Technology Conference*,(1996)

[3] Kouichi Yamada, Naofumi Sakai, Yoshiyuki Ishizuka and Kazunobu Mameno,*2001 Symposium on VLSI Circuits Digest of Technical PaperSK.*,(2001)

[4] Roy Scheuerlein, William Gallagher, Stuart Parkin, Alex Lee, Sam Ray, Ray Robertazzi and Willam Reohr,*ISSCC 2000*,(2000)

[5] Peter K. Naji, Mark Durlam, Saied Tehrani, John Calder and Mark F. DeHerrera, *SSCC 2001*,(2001)

[6] M. Durlam, P. Naji, M. DeHerrera, S. Tehrani, G. Kerszykowski and K. Kyler, *ISSCC 2000*,(2000)

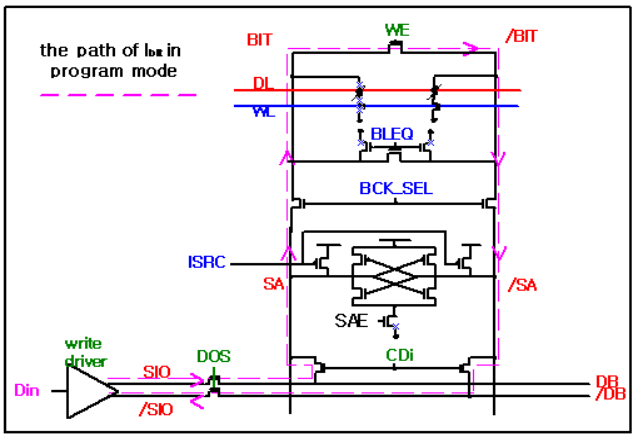

Fig 1. MRAM sensing circuit

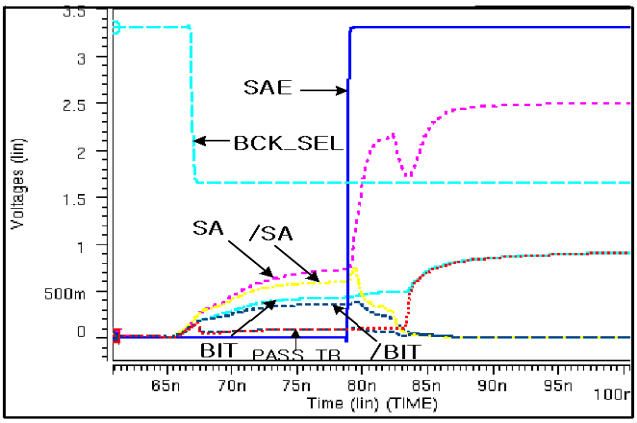

Fig 2. Simulated waveforms

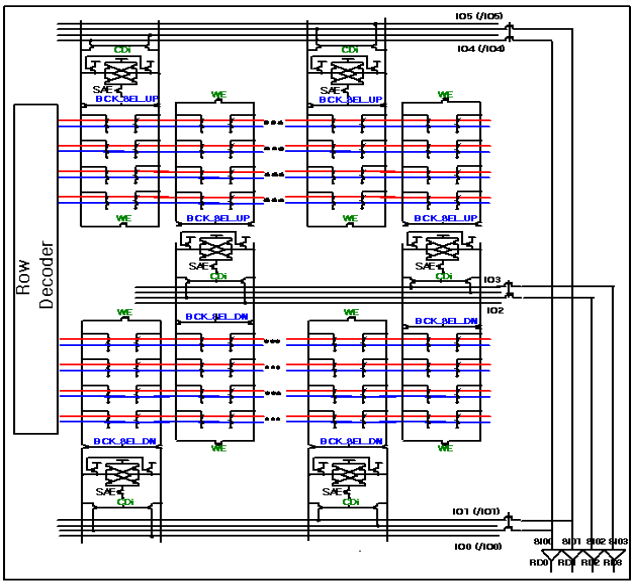

Fig 3. Array schematic

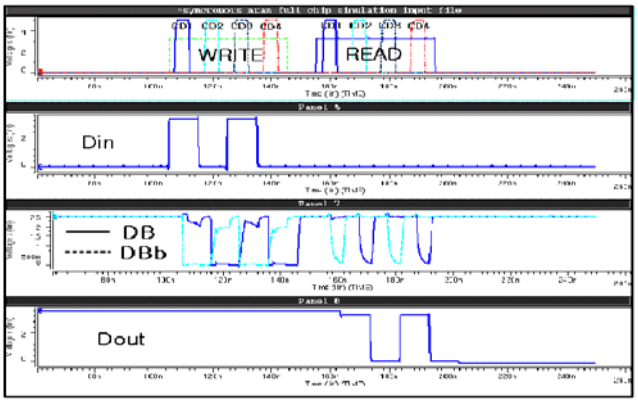

Fig 4. Full chip simulation

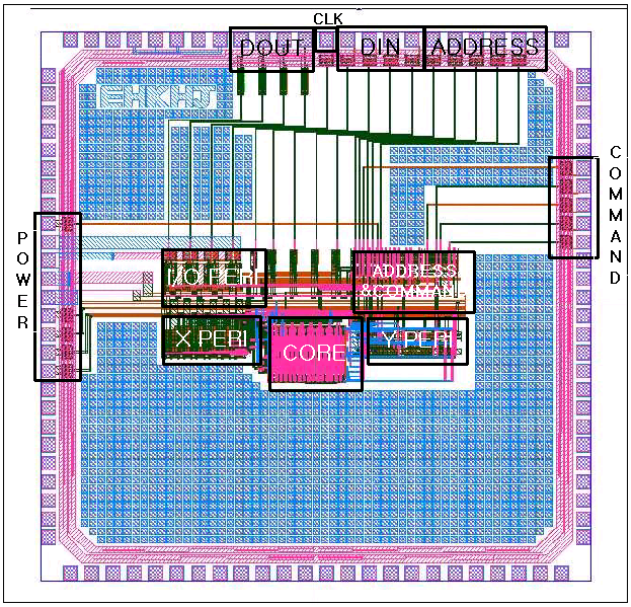

Fig 5. Full chip layout