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Dynamic Thermal Characterization and Modeling of Silicon Bipolar Junction Transistors using Pulsed RF Measurement System

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1. Introduction

Classical approaches make use of DC and S-parameters measurements in order to obtain I-V and high frequencies chracteristics of the transistors. However, DC measurements suffer from several drawbacks regarding the control of working parameters of the transistor. Especially for field -effect transistors (FETs) steady-state DC characteristics don't provide the correct RF characteristics due to trapping effects. Moreover, with the increasing current density of bipolar junction transistors (BJTs), the rise in junction temperature due to the dissipated power is becoming significant. To overcome these problems, pulsed measurement systems[1,2] were developed to pulse the bias of a device and measure the DC and RF characteristics before trapped charge or junction temperature can change appreciably. In this way, the measured data will not contain the trapping effect and self-heating effect. In this paper, DC and high-frequency characteristics of power Si BJTs with different emitter sizes will be shown based on pulsed DC and pulsed S-parameters measurements.

2. Device Characterization and Modeling

Pulsed DC and pulsed S-parameters measurements were performed using the Agilent 85124A pulsed RF modeling system.[2] The emitter areas of multi-finger Si BJTs under characterization are 0.6μm×32μm×3finger and 0.6μm×16μm×6finger and (0.6μm×16μm×1finger)×6cell. Measurements were made with Cascade microwave probes in the common-emitter mode. These devices were measured on wafer with G-S-G (Ground-Signal-Ground) microwave probes up to 15GHz using standard SOLT calibration procedure. The parasitics associated with the metal pads were removed by measuring both the dummy (metal without device) and the device and subtracting one result from the other in the y-domain. Figure 1 displays the pulsed profile of a BJT. The quiescent biases for base and collector were set to 0, while base and collector pulse biases were 1V and 4V, respectively. The base voltage and collector voltage were kept at constant value in the pulse duration. However, the collector current increases gradually with measured time due to self-heating effect. In the pulsed measurement, the device is allowed to cool down during the off time of the pulse period. So the self-heating effect can be eliminated as current sampled at short measurement delay time (≤1μs). As measurement time is long enough, the current saturates and the value approaches to that at static condition, so the self-heating almost reaches to static-state. To obtain stable signal and reduce the junction heating as low as possible, we choose 1μs as the measurement delay for isothermal measurement.

In this paper, the VBIC model parameters was extracted similar with Ref.[3] excepts the thermal resistance R_{th} and the thermal capacitance C_{th}. In this study, R_{th} can calculated by following formula :

$$R_{th} = \frac{Y_{22,SH} - Y_{22,noSH}}{D_2(I_C^2 + Y_{22,SH}P)} \quad (1)$$

where $Y_{22,SH}$ is the output conductance measured under CW(continuous wave) measurement which includes self-heating effect, $Y_{22,noSH}$ is the output conductance measured under pulsed mode measurement which includes self-heating effect, P is the power consumption, $D_2=(\partial I_C/\partial T)/I_C$ can be extracted from Gummel Plot measured under different temperature. Finally, C_{th} can be calculated based on the shape of collector current (as shown in Fig. 1), here collector current can be expressed as: [4]

$$I_C(t) = I_{C,i} + (I_{C,s} - I_{C,i})\left[1 - \exp\left(-\frac{t}{\tau_{th}(I_{C,s}/I_{C,i})}\right)\right] \quad (2)$$

where $I_{C,i}$ and $I_{C,s}$ is the initial value and stable value, respectively.

3. Results and Discussion

Figure 2 shows the cutoff frequency f_T of a Si HBT as a function of collector current at different measurement delays. Because of the bandgap narrowing effect in heavily doped emitter region, the bandgap difference ΔE_g between emitter and base is negative. Since the current gain is proportional to $\exp(\Delta E_g)/kT$, where k is Boltzman's constant and T is temperature, the higher junction temperature will make a increase of the current gain, As a result, the measured cut-off frequency at 50μs is higher than that at 1μs when the applied current is relatively small. However, the thermal effect reduces the saturation velocity and the critical current at which the Kirk effect takes place [5], the fall-off of the cut-off frequency begins earlier for 50 μs measurement delay. That is the reason measured cut-off frequency at 50 μs is higher than that at 1μs in the high current region. Table 1 summarized the collector current density difference ΔJ_C, the cutoff frequency difference Δf_T, and the maximum oscillation frequency difference Δf_{max} of three different Si BJTs biased at V_{CE} = 4V, V_{BE} = 1.1V between CW and pulsed-mode measurement. It seems that the thermal interaction between fingers makes higher ΔJ_C thus higher junction temperature in devices with more fingers. To reduce the thermal interaction in a multi-finger BJT and thus reduce the saturation velocity and the critical current at which the Kirk effect takes place, we can divide all the emitter

fingers into several sub-cells. As shown in Table 1, transistor with six sub-cells has lowest ΔJ_C, Δf_T, and Δf_{max} than those without sub-cells at same emitter area. Table 2 summarized the extracted R_{th} and C_{th} of three Si BJTs with the same emitter area. Transistor with sub-cells has lower thermal resistance than those without sub-cells. Hence, parallel interconnected sub-cells are preferable to large multi-finger layouts for Si BJTs. Figures 3 and 4 compare the VBIC modelling results of DC and AC data for the Si BJT with emitter area = 0.6μm×32μm×3finger. Measurement using ATN LP1 Load-Pull system and HB simulation using Agilent ADS are also adopted for VBIC model validation in linearity analysis and the results are shown in Fig.5 and Fig.6. All the simulation results show very good agreement with the measured data.

5. Conclusions

Electrical characteristics of the Si BJTs with different emitter design are shown and discussed based on static and pulsed-mode measurements. Parallel interconnected sub-cells are preferable to large multi-finger layouts for Si BJTs. DC, AC and linearity performance of the Si BJT is also validated using VBIC model and the simulation results shows good agreement with the measured data.

References

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Table 2: Thermal resistance R_{th} and thermal capacitance C_{th} of three Si BJTs with the same emitter area.

Emitter Area	R_{th}(°C/W)	C_{th} (nJ/°C)
0.6μm×32μm×3	286	8.07
0.6μm×16μm×6	290	7.43
(0.6μm×16μm×1)×6sub-cells	254	7.43

Table 1: Collector current density difference ΔJ_C, cutoff frequency difference Δf_T, and maximum oscillation frequency Δf_{max} of Si BJTs with different emitter design. V_{CE} = 4V, V_{BE} = 1.1V.

Emitter Area	J_C (CW) (μA/μm²)	J_C (pulse) (μA/μm²)	ΔJ_C (μA/μm²)	f_T (CW) (GHz)	f_T (pulse) (GHz)	Δf_T (%)	f_{max} (CW) (GHz)	f_{max} (pulse) (GHz)	Δf_{max} (%)
0.6μm×32μm×3	452.1	424.3	27.8	13.2	14.2	7.3	18.4	19.2	4.3
0.6μm×16μm×6	458.3	433.3	25.0	9.5	10.3	8.1	15.3	16.0	4.5
(0.6μm×16μm×1)×6sub-cells	411.5	396.7	14.8	17.3	18.2	5.1	19.4	19.9	2.5

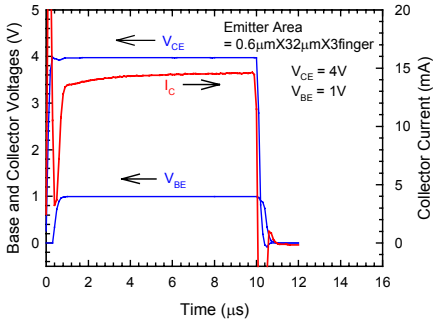

Fig. 1. Base voltage, collector voltage and collector current pulse shapes of a BJT.

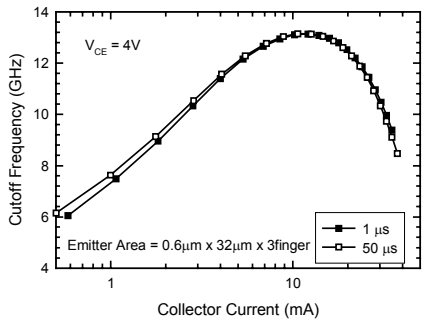

Fig. 2 Cutoff frequency as a function of collector current for a Si BJT under different pulsed-mode measurement.

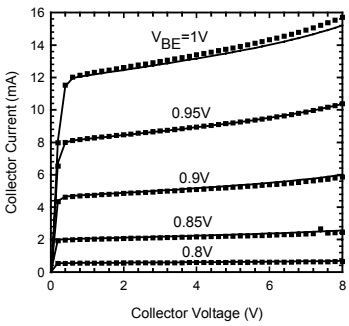

Fig. 3 Measured and simulated current-voltage characteristics under forward operation of the Si BJT with emitter area = 0.6μm×32μm×3finger.

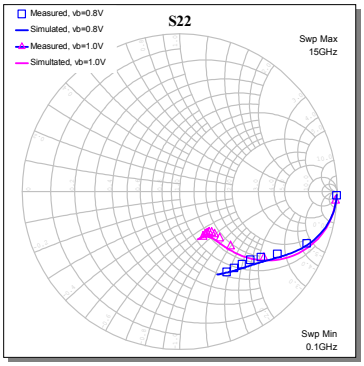

Fig. 4 The modeling results of S11 and S22 traces for the Si BJT biased at V_{BE} = 1V and V_{CE}= 2V. The emitter area is 0.6μm×32μm×3finger.

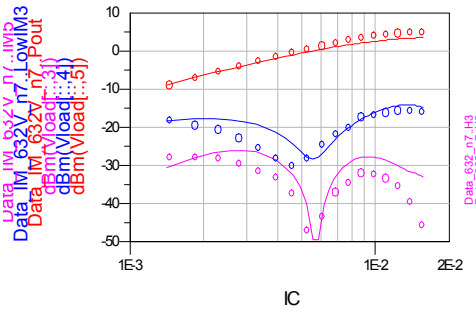

Fig. 5 Modeled and measured current dependence of the output power at the fundamental (2.4GHz), 3rd order and 5th order inter-modulation frequencies. V_{CE} = 3V, Pin = -7dBm,Tone spacing = 1MHz. The emitter area of the Si BJT is 0.6μm×32μm×3finger.

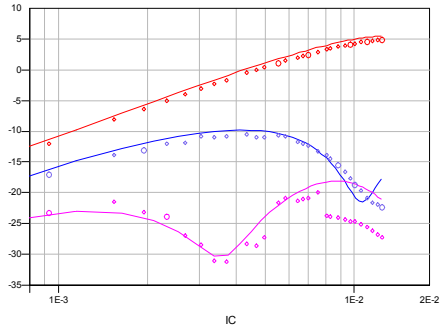

Fig. 6 Modeled and measured current dependence of the output power at the fundamental(2.4GHz), second and third harmonic frequencies.V_{CE} = 3V, Pin=-7dBm. The emitter area of the Si BJT is 0.6μm×32μm×3finger.