A Study of ESD Protection under Pad Design for Copper-Low K VLSI Circuits

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1. Introduction

An electrostatic discharge (ESD) under pad design is proposed for novel copper-low K circuits design. With our design, the density of devices and pad could be significantly improved. Moreover, no ESD, latch-up and yield loss problems are caused. The design is very useful in VLSI circuit with copper-low K interconnections for sub-0.1um device era. ESD dominates few percents of yield loss in integration circuits. Thus, a robust ESD protection circuit is very important in IC design. Recently, it is found that the designing of ESD protection circuit becomes more challenging as the dimensions of devices shrink, particularly for CMOS technologies [1]. Those issues are caused from two aspects; one is the nature of nano-scaled devices and the other one is due to the requirement of ultra-large scaled circuits [2]. The ESD robustness caused from devices scaled down had been discussed in many works; therefore, a circuit consideration for ESD protection design is taken in this paper. In circuit design of view, the challenges could be caused from two ways. First, the parasitic capacitance of the ESD protection devices will degrade the benefit of high switching speed in nano-devices. Second, unable to scaling down the size of ESD protection device will lower the device density of IC. The second item is paid much attention that makes the cost of ESD protection circuit increasing. Moreover, this characteristic will also limit pad number of chip design. To improving the density of both devices and pads, ESD protections circuit under pad design is proposed and demonstrated for copper-low K generations for the first time. It is found that, without degrading ESD robustness, the area efficiency of chip could be largely improved; furthermore, higher pad density will be also achieved.

2. Circuit design and fabrication

Fig. 1 exhibits the proposed circuit for ESD protection. The schematic is total the same with the conventional circuit design for ESD protection. Though with the same circuit schematic, they are very different in the layout and cross-section views. Figs. 2 and 3 show the topologic views of both the conventional and under pad structure. For the pad and ESD protection devices are occupied at the same area of the under pad design, the under pad one has a much better area efficiency than the conventional one. More details could be observed from the cross section view shown in the figure 4 that we put our protection devices under the bonding pads. In comparing with the conventional pad structure presented in Fig. 5, we take the advantage of the non-used area under pad. It is no doubt that the under pad structure did improve our area efficiency in circuit design. In this experiment, a 90nm CMOS technology with copper-low K interconnections is used to fabricate our under pad structure. There are seven copper metal layers and one poly-silicon layer in circuit design and manufacture. The ESD robustness is tested by using human body model (HBM) of industry standard.

3. Pad density issues

For many high-end applications, a large number of pads are always required. Thus, the pad density could be also taken in count when developing an ESD protection circuit. Fig. 6 shows the stagger pad structure for high-density pad design. By using the design, we can increase about 50 percents of pad density. However, the improvement is limited. For the under pad structure, considering the cell width of protection devices is unnecessary, we can make our pad number as large as we wanted. Moreover, for the nature of under pad structure, the design is especially suitable for flip chip design. Fig. 7 is a topologic view for under pad I/O pad array.

4. Bond yield test

In using the under pad protection structure, the mechanical stress damage during wire bonding should be considered. Table 1 reports an ESD testing for under pad and convention ESD device. In this experiment, 30 samples are bonded and tested to study the stress affects on the devices characteristics. Fig. 8 shows the normal IV characteristics of the test devices. In comparing with the pre-bonding IV curves and post-bonding ones, we can obtain bonding yield. The bonding yield can be observed from Fig. 9 that no matter how many layers of pad metal are designed, no yield loss is found. Fig. 10 is an ESD testing for under pad and convention ESD device.

5. ESD robustness and latch-up test

The ESD robustness testing is also performed on our under pad structure. It could be found that all under pad sample could pass 3KV. It is better than the conventional structure. The uniform turn-on characteristic could be the major factor that makes ESD robustness improvement. By our developed TCAD simulator [3], it is found that turn-on uniformity could be improved by under pad design. Moreover, the under pad structure could also pass the latch-up testing as shown in Table 2.

6. Conclusions

The ESD protection under pad structure is proposed and demonstrated having a high efficiency in area usage, a higher pad density no any other site effects. This structure is very useful in novel integration circuit design.

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References

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Fig. 1. Schematic for ESD protection circuit.



ESD protection circuit.



ESD protection circuit.



Fig. 5. A cross-section view for conventional ESD protection circuit.



Fig. 2. A topologic view for conventional Fig. 6. A topologic view for stagger I/O pad array.





Forward

Voltage

Jurrent

Reverse





pad and conventional ESD device.

Package samples Bonding pass samples 35 30 <u></u>25 15 10 5 0 M3 M4 M5 traditional

Fig. 9. Bond yield testing for under pad and convention ESD device.



Fig. 10. An ESD testing for under pad and convention ESD device.

	HBM (KV)		
Description	M3	M4	M5
Metal width 30um	3.1	4.8	4.3
Metal width 20um	5.1	5.1	5.4
Metal width 15um	3.3	3.9	3.9
Metal width 10um	3.8	3.5	5.4
Metal width 5um	3.6	4.1	4.6
Metal width 2um	3.6	3.3	3.8

Table 1. An ESD testing for under pad and convention ESD device.

Trigger Mode	Test Pin	Sample Size
+ IT	I/P	200mA/4
- IT	I/P	200mA/4
VDD-VSS		6.6V/4

Fig. 4. A cross-section view for under Fig. 8. The IV characteristic for under Table 2. The latch-up testing for under pad and convention ESD device.

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