Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 676-677

P13-2

Thickness Dependent Device Operation of Sublimed Molecular Field-Effect Transistors

S. Hoshino*, M. Yoshida, S. Uemura, T. Kodzasa, T. Kamata, and K. Yase

Photonics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Higashi, Tsukuba, Ibaraki 305-8565, Japan
Phone: +81-29-861-4516 E-mail: s.hoshino@aist.go.jp

1. Introduction

To gain insights into the optimal device structure that enables efficient operation of organic field-effect transistors (FETs) is one of the important steps toward their practical use. This paper investigates dependence of the active layer thickness on device characteristics using typical sublimed molecular film-based FETs to provide a detailed discussion in this regard. We revealed that the device characteristics of our bottom-contact FETs based on Cu(II) phthalocyanine (CuPc) varied depending on the thickness of the CuPc layer, and the results suggested that the FETs had an optimum active layer thickness for efficient device operation at around 80 nm in this device configuration.

2. Experiments

Figure 1 shows the device structure of the FETs used in this study together with the chemical structure of CuPc. We prepared devices with a CuPc layer of 40, 50, 80, 100, 150, 250, and 400 nm, and operated them in a vacuum at room temperature. The device fabrication and the measurement procedures were described in detail in our recent paper [1].

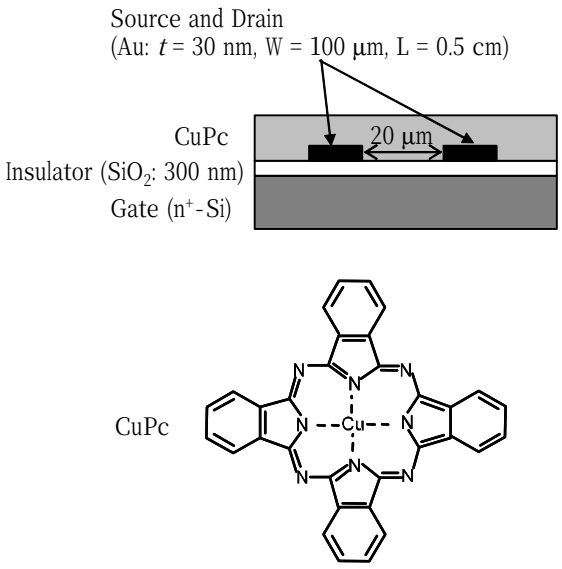

Fig. 1. Device structure of the CuPC-based FETs and the chemical structure of CuPc.

3. Results and Discussion

All the FETs used in this study exhibited the operating charac teristics of an enhancement mode *p*-channel FET except for 400-nm device, for which we observed negligible gain from the gate field. A typical output profile is shown for the 80-nm FET in Fig. 2. The drain current-drain voltage (I_d-V_d) curves consisting of linear and saturation regions were commonly found in the other thinner and thicker FETs. The on-state I_d, however, reached its highest value in the 80-nm device and those of the other devices were lower in both the linear and saturation regions if we compared at constant drain and gate voltages. This implies that the CuPc layer thickness affects the device performance of the bottom-contact FETs.

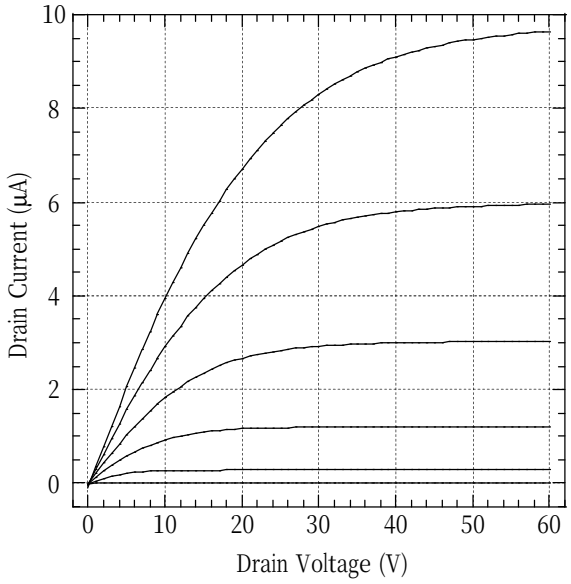

Fig. 2. I_d-V_d characteristics of the FET with a CuPc layer of 80 nm measured at various V_gs.

To understand the thickness dependence of the device performance quantitatively, we derived field-effect mobility (m) by analyzing the transfer characteristics at the saturation region. We found there was a linear relationship between the square root of I_d and V_g with the exception of the low V_g region, suggesting that the I_d at the saturation region of these FETs was modulated in accordance with the basic operation regime established for insulator-gate FETs [2]. The m s shown in Figs. 3 ranges approximately from 10^{-4} to 10^{-3} $cm^2/V•s$, and well describes the thickness dependent device performance predicted from the output I_d; the m is highest for the 80-nm device ($3.5×10^{-3}$ $cm^2/V•s$) and fell as the CuPc layer becomes thinner or thicker.

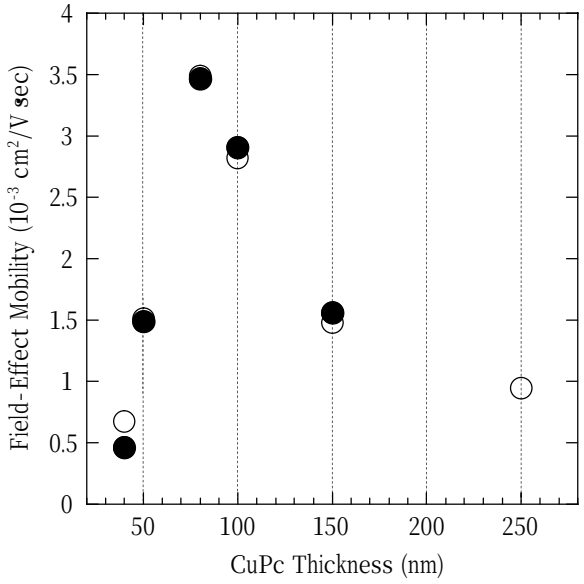

Fig. 3. Variation in the field-effect mobility (m) with the CuPc layer thickness. The Open and filled circles represent m calculated from the output characteristics in the saturation and linear region respectively. Each m was obtained from the I_d values at V_d = -60 V (saturation region) and the I_d-V_d profiles at V_g = - 50 V (linear region), respectively.

Next we analyzed the output characteristics in the linear region, where the electric field between the source and drain electrodes is lower than that in the saturation region. As shown in Fig. 3, the ms obtained from the linear region (m_{lin}) had almost the same thickness dependence as that found for the m at the saturation region (m_{sat}). Fig. 3 displays that the difference between m_{lin} and m_{sat} ($m_{lin}<m_{sat}$) is marked in both the 40- and 250-nm devices whereas it was very small for the others, in particular negligible for the 80-nm FET. We compared the I_d-V_d profile of the former and latter FETs through its change in differential drain conductance ($\partial I_d/\partial V_d$) with V_d. As V_d was swept to negative direction, the $\partial I_d/\partial V_d$ varied with peaking at around V_d = -10 V for the 40- and 250-nm devices. By contrast, it decreased monotonously in the 80- and 100-nm FETs. We conclude that the m is source-drain field dependent at the thicknesses having the inefficient device operation whereas the dependence is quite weak at that around 80 nm. It is likely that the field dependent m originates from a significant trapping effect on the carrier transport in the channel region, where the hole conduction may be predominated by the field dependent carrier hopping process such as Poole-Frenkel type carrier emission [3].

We believe that the variation in the trapping effect cannot be explained simply by a morphological change in the conduction channel, where imperfect coverage of the active layer must be improved through an increase in film thickness because we observed the marked difference between the m_{sat} and m_{lin} for the thinner and thicker CuPc layer. Instead, we estimate that the trapping effect varies its influence on the hole conduction through a change in the location of the conduction channel, consequently the thickness dependence of the device performance occurs. In the FET with a thin (~ 40 nm) or thick (> 250 nm) CuPc layer, the chief carrier conduction pass within the conduction channel may be in the vicinity of the CuPc film surface and/or the gate insulator interface, where carrier trap density is apt to be higher than that in the bulk. On the other hand, we suspect that balance between the thickness and the longitudinal potential profile in the active layer must be appropriate for placing the conduction pass far off these boundary parts at around 80 nm.

4. Summary

We investigated the thickness dependence of the device characteristics of CuPc-based bottom-contact FETs. We confirmed that the operating performance varied depending on the thickness and the best device performance was obtained for FETs with a CuCp layer around 80 nm thick. We hypothesized that the thickness dependence was responsible for the difference in the hole trapping effect, which might be varied by the position of main carrier conduction pass determined by a correlation between the thickness and the longitudinal potential profile in the active layer. We are currently attempting to clarify the device physics behind this thickness dependence to reveal whether the thickness dependence is peculiar to these CuPc-based devices or generally observable in organic FETs with the same configuration.

References

[1] S. Hoshino, T. Kamata, and K. Yase, J. Appl. Phys. **92**, 6028 (2002).
[2] For a review, see C. D. Dimitrakopoulos and D. J. Mascaro, IBM J. Res. Dev. **45**, 11 (2001).
[3] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981).