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Efficient Improvement of Hot-Carrier-Induced Degradation for Sub-0.1μm CMOSFET

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Abstract - The effect of post-thermal annealing (PA) after halo implantation on the reliability of sub-0.1μm CMOSFETs was investigated. We found that the control of annealing time is more efficient than that of annealing temperature with respect to improving the hot-carrier-induced device degradation. The best results of device performance were obtained with post-annealing treatment performed at medium temperatures for a longer time.

Introduction

Engineering channel dopant profiles obtained by localized halo implantation have been extensively used in sub-0.1μm CMOSFETs [1]. Owing to low diffusion constant, indium (In) has been successfully used in fabricating abrupt and shallow halo profiles for deep submicron nMOSFETs. Unfortunately, interstitial Si caused by the In ion implantation results in the increase of leakage current and the degradation of device performance [2]; thus, a post-thermal annealing (PA) treatments after In-halo implantation are proposed to solve these problems. Besides, the PA will also affect pMOSFET's performance. In this work, the effect of PA on hot-carrier-induced device degradation was investigated for the sub-0.1μm CMOSFETs.

Experiments

Sub-0.1μm CMOSFET was fabricated with 2nm nitride gate oxide using dual gate twin-well process. After gate patterning, n/p source/drain extension were formed with arsenic (As) as well as Boron (B) implantations in respectively. Then tilted-angle halo-implantation at 20~30 degree with B (at 10~30KeV, 2~5 x 10^{13} cm^{-2}) as well as In (at 120~180KeV, 1~3 x 10^{13} cm^{-2}) for nMOSFET, and As (at 110~130KeV, 2~4 x 10^{13} cm^{-2}) for pMOSFET. After halo implantation, various post annealing were employed at 900 to 1050^{o}C with various annealing time. Then n^{+}/p^{+} deep source/drain junction was formed with As and B ion implantation in respectively. Finally, wafers were processed through $CoSi_2$ salicidation process and a standard backend flow to completion. To investigate the HCE, device stressing and measurements were made on a probe station at various drain voltages ($|V_D|$ = 1.2~2.0V) and gate voltages ($|V_G|$ = 0~1.8V) with a stressing time ranging from 0 to100min.

Results and Discussions

As shown in previous study [3], in comparison with B-halo structure, the margin of device's punch-through can be improved with In-halo structure because of the localized junction profile; thus, In-halo is able to suppress the nMOSFET's SCE down to sub-0.1μm channel length, as shown in Fig. 1. Figure 2 shows intrinsic transconductance (G_m) versus with DIBL distribution, it is worth noting that the mobility of In-halo nMOSFET was better than that of B-halo device especially as L_{eff} less than 0.1μm. Since a large amount of Si interstitial, which generated by As-extension implantation and enhanced by In-halo implantation, can react with In dopant more efficiently, resulting in a more pronounced deactivation and causing an accelerated V_{th} roll off for short-channel devices. Thus, PA was proposed to remove these Si interstitial and suppress the TED phenomena. In this work, Si interstitial can be removed by an annealing especially at lower temperature and longer time without degrades device's SCE. Although the localized In-halo dopant located only around extension junction without degrading the device's driving capacity [3], the hot-carrier effect of In-halo device was still a problem and became more serious as device dimension decreases. In comparison with B-halo nMOSFET, the hot-carrier-induced G_m degradation of In-halo nMOSFET becomes more serious after hot-carrier stress especially at higher gate voltage, as shown in Fig. 3. For In-halo nMOSFET, the abrupt and shallow junction profile increases drain electric field and enhances high impact-ionization rate of channel carrier, thus aggravates the hot-carrier effect. It is apparently that B-halo device shows lesser junction leakage than In-halo device, as shown in Fig. 4. According to the results of B. Yu *et.al* [1], B-halo nMOSFET shows normal recombination-generation junction leakage happen, while high localized dose of In-halo nMOSFET indicates that the drain to halo (body) band-to-band tunneling current starts to present. This tunneling leakage can be considerable contributor to the device's off-state leakage current (I*do*), resulting in higher device's I*do* with In-halo structure. The swing degradation indicates the creation of interface traps resulting in a threshold voltage shift [4]. The gate-induced drain leakage (GIDL) in both nMOSFETs at a negative gate bias of V_G = -0.5V was also increased. It has been reported that GIDL is a direct result of the generation of interface states; thus, the largest degradation in I_{Dsat} coincides with the largest increase in interface state density. In comparison with B-halo nMOSFET, the In-halo nMOSFET subthreshold characteristic shows larger I*do* and GIDL. Furthermore, the gate leakage of In-halo device was larger than that of B-halo device, and will be enhanced after hot carrier stress, as shown in Fig. 5. With appropriate PA, the In-halo device's subthreshold characteristic can be improved and GIDL was suppressed apparently, as shown in Fig 6. The device's subthreshold swing and I*do* can be improved especially at 900^{o}C with longer time annealing. Fig. 7 reveals that the hot-carrier-induced saturated drain current (I_{dsat}) degradation of In-implanted nMOSFETs was more serious than that of B-implanted nMOSFETs. With an appropriate PA, the I_{dsat} degradation of all In-implanted devices was improved and lowers than that of B-implanted devices. For In-halo nMOSFET, very low drain degradation (<3%) can be obtained by PA at medium temperature with enough annealing time. Because the impact ionization caused by electron can be suppressed with appropriate PA, In-halo shows longer lifetime than B-halo nMOSFET especially at stress voltage larger than 1.5V, as shown in Fig. 8. For pMOSFET, Si interstitial still happens after As-halo implantation. These interstitial will degrades device performance and enhances hot carrier effect. Fig. 9 shows G_m of pMOSFET was decayed apparently after hot carrier stress. Thus, PA is necessary to improve this problem. However, pMOSFET's characteristic will be degraded during PA due to the out-diffusion of channel doping-profile, causing threshold voltage (V_t) shift especially at 1000^{o}C annealing. In this work, hot-carrier-induced G_m degradation can be improved especially with PA using 900^{o}C and longer time without V_t shifting. And the devices subthreshold swing as well as gate leakage were also improved and has no degradation apparently after hot carrier stress, as shown in Fig. 10 and 11 respectively. With appropriate PA, the hot-carrier-induced I_{dsat} degradation of As-halo pMOSFET can be improved, as shown in Fig. 12. Very low drain degradation (<1%) was obtained by PA at 900^{o}C with enough annealing time.

Conclusion

In this work, post thermal annealing effect impact on hot-carrier-induced reliability of 0.1μm CMOSFET was inspected. For In-halo nMOSFET as well as As-halo pMOSFET, hot-carrier-induced device degradation can be improved by post annealing especially at medium temperature with long time annealing without degrading device's performance.

Acknowledgement

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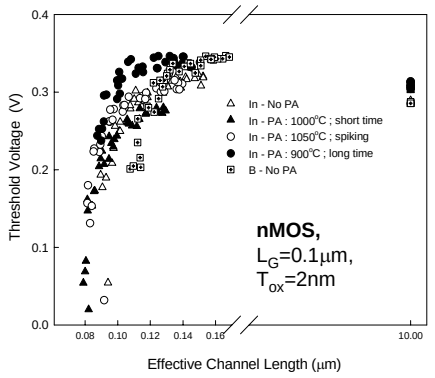

Fig. 1 V_{th} *vs.* effective channel length for In-halo and B-halo nMOSFETs.

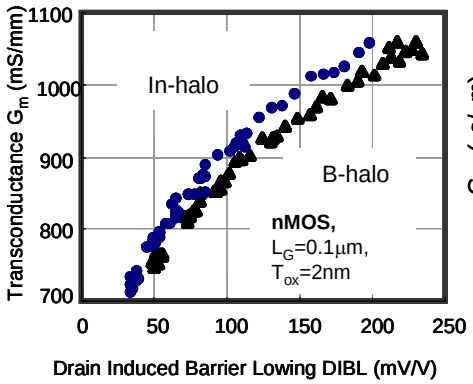

Fig. 2 G_m *vs.* DIBL for In-halo and B-halo nMOSFETs.

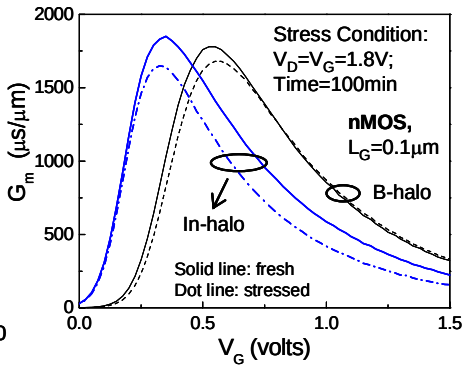

Fig. 3 G_m *vs.* V_G for In-halo and B-halo nMOSFETs before and after hot carrier stress.

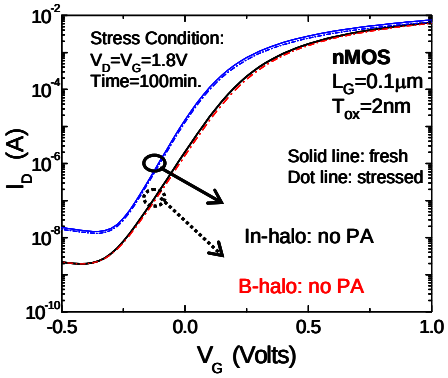

Fig. 4 I_D *vs.* V_G for In-halo and B-halo nMOSFETs before and after hot carrier stress.

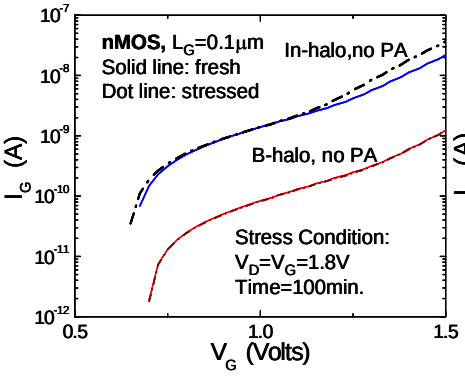

Fig. 5 I_G *vs.* V_G for In-halo and B-halo nMOSFETs.

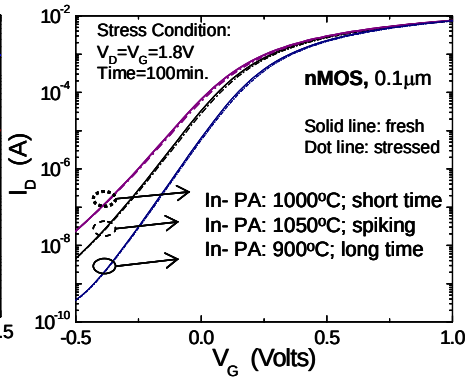

Fig. 6 I_D *vs.* V_G for In-halo and B-halo nMOSFETs before and after hot carrier stress with various post annealing.

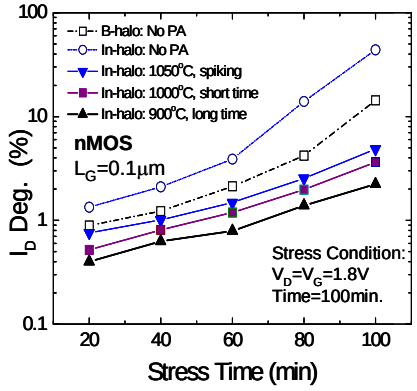

Fig. 7 I_{DSAT} degradation *vs.* stress time for nMOSFET under various post annealing.

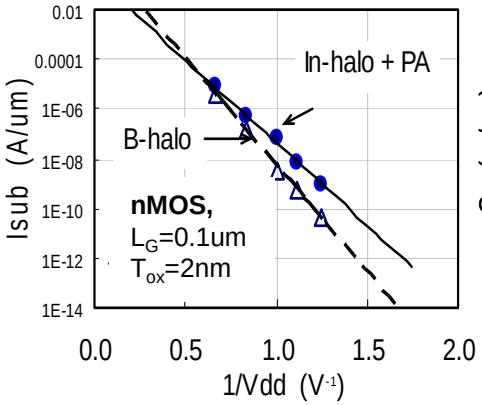

Fig. 8 I_{sub} *vs.* stress voltage for In-halo and B-halo nMOSFETs.

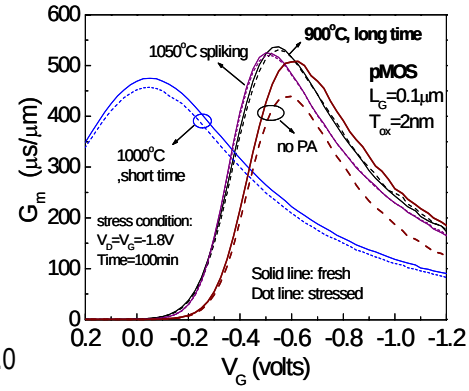

Fig. 9 G_m *vs.* V_G for pMOSFETs before and after hot carrier stress.

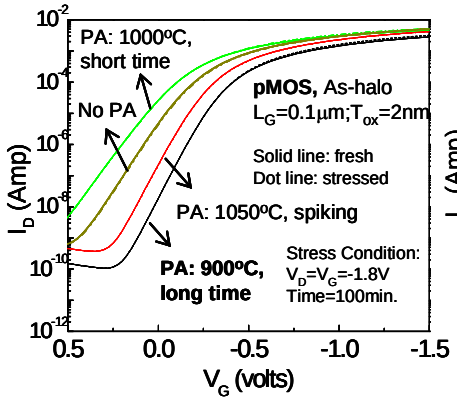

Fig. 10 I_D *vs.* V_G for pMOSFETs before and after hot carrier stress.

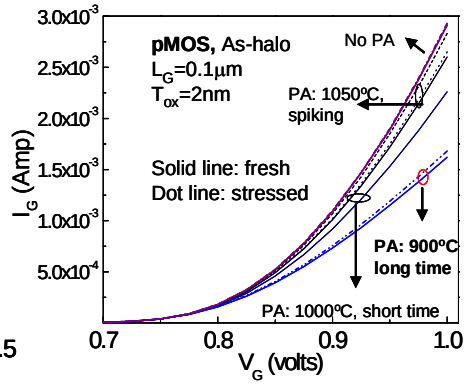

Fig. 11 I_G *vs.* V_G for pMOSFETs under various post annealing.

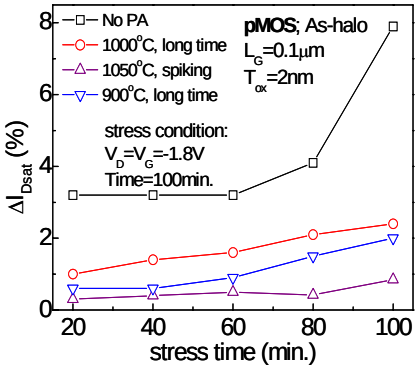

Fig. 12 I_{DSAT} degradation *vs.* stress time for pMOSFET under various post annealing.