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On-current Modeling of poly-Si TFT

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1. Introduction

It is well known that the characteristics of polycrystalline silicon (poly-Si) TFTs (thin film transistors) such as the on-current and mobility are significantly decreased by their inherent trap states in grain boundary as well as in interface [1][2][4]. Most of previous work regarding to characterization of poly-Si TFT has been focused on the grain boundary traps rather than interface traps. However, the interface traps should be carefully considered in order to accurately investigate the device characteristics. The purpose of our work is to propose a new on-current model including interface traps as well as grain boundary traps. We have extracted the interface trap charges from experimental data using our new model equation. Our model accurately predicts the I-V characteristics of poly-Si TFT.

2. The effect of interface traps on the mobility

We fabricated TFTs with various interface properties due to process variation. We measured 20 TFTs of which the grain size is almost identical. The on-current is defined as the drain current at V_{gs} of 10V and V_{ds} of 10V.

Fig.1 shows the relation between subthreshold slope and On-current. The drain current is decreased as the shubthreshold slope of TFT increases as shown in Fig.1. It is well known that the subthrshold slope is mainly influenced by interface trap and the drain current is reduced by the mobility degradation [2]. The result in Fig.1 indicates that the interface trap charges strongly affect the mobility degradation. In order to accurately estimate the relationship between the mobility and grain boundary trap density, we evaluated four TFTs chosen in Fig.1. The evaluation was carried out with well-known equation (1) [1][3][4].

$$\mu_{eff} = \mu_o \exp(-E_b / KT) \quad \text{.....(1)}$$

Fig.2 shows that the band mobility is directly related to subthreshold slope, which indicates that the band mobility may contain the parameter controlled by interface states.

3. Model equations and Results

The proposed model equation consists of two basic terms, which are thermionic emission and UT mobility equation [1][6]. The thermionic emission is used for the grain boundary trap states and UT model is for interface trap charges [6]. The basic formula is shown in equation (2).

$$1/\mu_{eff} = 1/\mu_G + 1/\mu_{GB} \exp(-E_b / KT) \quad \text{.....(2)}$$

The equation (2) is slightly modified for poly-Si TFT by means of several assumptions. First, it is assumed that the mobility of intra-grain is identical to that of conventional MOSFET. The mobility terms are expressed as a function of a vertical effective electrical field, E_{eff}. The E_{eff} is represented by two terms; inversion charges and depletion charges [6]. In our proposed model, the grain boundary trap charge is substituted for the depletion charge because the channel is intrinsic and the grain boundary trap is also depleted under inversion condition. A thickness of inversion layer is evaluated with the modified E_{eff}. The thickness is used for intra-grain mobility as well as potential barrier induced by grain boundary trap. A carrier transport in grain boundary is assumed to be only thermionic emission. The grain boundary mobility is expressed as thermal collection velocity and grain size as shown in equation (3).

$$\mu_{GB} = L_G v_c / V_T \quad \text{.....(3)}$$

A relation between channel length and grain size is also considered. When the channel length of TFT approaches the grain length, the grain boundary effect may be reduced because the channel has one or two grain boundaries. However, the equation (2) cannot exhibit the relation between channel length and grain length. The effect of grain size has been considered as equation (4) [7].

$$\frac{L_G + L_{GB}}{\mu_{eff}} = \frac{L_G}{\mu_G} + \frac{L_{GB}}{\mu_{GB} \exp(-E_b / KT)} \quad \text{.....(4)}$$

For equation (4), the grain boundary length should be measured or evaluated. It is rather difficult to measure the length so that we evaluated the length from numerical method. When the grain boundary traps are assumed to be full occupied with inversion charges, the depletion with (W_d) is expressed as equation (5). The W_d is substituted for L_{GB} in equation (4).

$$\frac{Q_i}{qz} W_d = N_t \quad \text{.....(5)}$$

Finally, the intra-grain mobility is also modified to consider the interface charge. The poly-Si TFT has larger interface trap states than in conventional MOSFETs. It may be considered that the interface trap states are fully occupied with electrons under on-state (above threshold) so that the effective mobility is affected not only by the fixed trap charge but also by the interface trap state. The mobility term related to interface charge is expressed as equation (6) for above consideration.

$$p = 0.09 + 4.5 \times 10^{-8} \frac{N_{it} (= N_f + n_{it})}{N_I^{0.25}} \quad \text{.....(6)}$$

The 4 chosen TFTs were evaluated with the proposed

equations. Fig.3 shows the comparison between experimental data and simulated data. Simulated results were well fitted with experimental results. The numerical data indicate that the extracted interface trap (N_{it}) increased with decrease of subthreshold slope of TFTs and that the number of grain boundary trap (N_t) in each TFT was almost identical. The extracted parameters support the results in Fig.1 and Fig.2.

4. Conclusion

The new on-current model equation which includes parameter induced by the interface trap charges is proposed. The band mobility of ploy-Si TFTs is found to be critical dependent of interface states. The results from our model successfully explain that increase of the mobility is originated from reduction of the interface traps in case of same grain size. The proposed model may be useful to characterize and to design poly-Si TFT.

References

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Appendix : Parameters & Equations

μ_G	intra-grain mobility
μ_{GB}	grain boundary mobility
μ_o	band mobility
μ_C	bulk mobility
μ_S	interface scattering mobility
μ_k	surface scattering mobility
E_b	grain boundary potential barrier
N_t	number of grain boundary trap per unit area
N_I	number of inversion carrier unit volume
n_{it}	number of interface trap per unit area
N_f	number of fixed trap charge per unit area
N_{it}	total number of interface charge per unit area
Q_i	inversion charge per unit area
k_s	surface roughness coefficient
p	Fuchs scattering factor
z	inversion layer width including quantum broadening effects
v_c	thermal velocity
V_T	thermal voltage

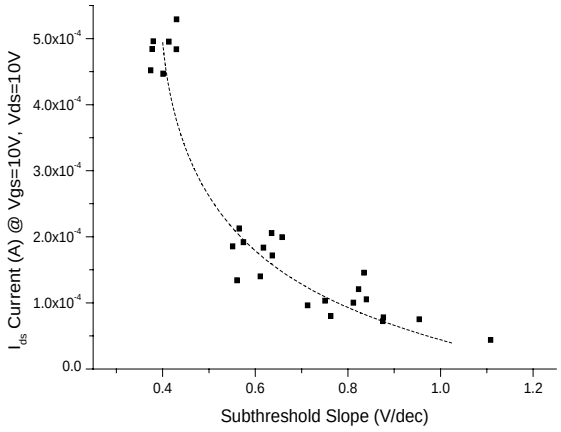
$$E_b = \frac{z(qN_t)^2}{8\varepsilon_{si}Q_i} \quad \text{(A-1)}$$

$$E_{eff} = \frac{1}{\varepsilon_{si}}\left(\frac{1}{3}Q_i + qN_t\right) \quad \text{(A-2)}$$

$$\mu_G = \left[\frac{1}{\mu_C} + \frac{1}{\mu_s} + \frac{1}{\mu_k}\right]^{-1} \quad \text{(A-3)}$$

$$\mu_G = \left[\frac{1}{1150} + \frac{3.2\times10^{-9}p}{z} + \frac{E_{eff}}{k_s}\right]^{-1} \quad \text{(A-4)}$$

$$z = \frac{0.039}{E_{eff}} + \frac{1.24\times10^{-5}}{E_{eff}^{0.33}} \quad \text{(A-5)}$$



Fig,1. I_{ds} Current of TFTs with the variation of subthreshold slope

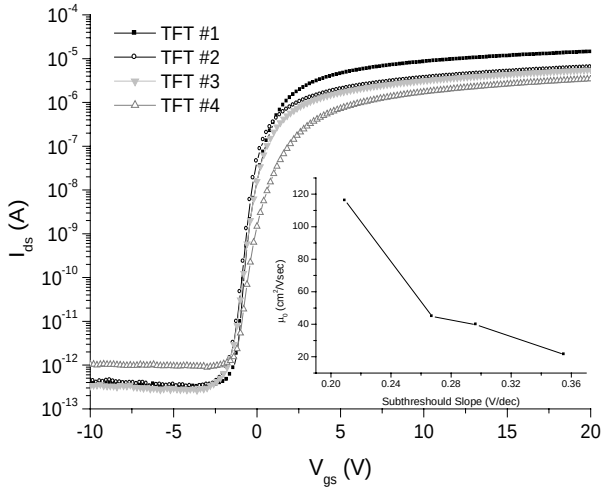


Fig.2. The band mobility of TFTs with the variation of subthreshold slope. (TFT #1, #2, #3 and #4 are chosen in Fig.1. W/L=20/8, LDD=1.1 ㎛, Vds=0.1V)

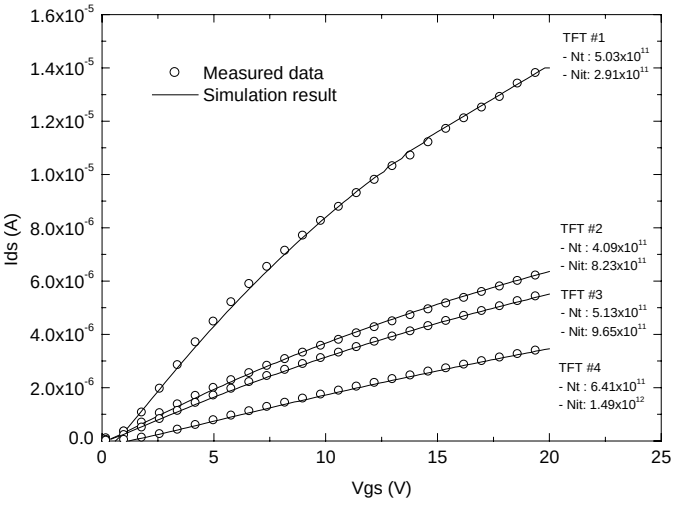


Fig.3. Comparison modeling results with experimental results