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# Split Gate Engineering for RF/Analog Application In Sub 50 nm NMOSFET

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## I Introduction

Deeply scaled CMOS has enabled many high performance SOC applications. In addition to high speed digital transistors, sub-130nm CMOS can be an excellent choice for radio-frequency (RF) wireless communications [1]. These RF MOSFETs can be integrated with digital circuits, resulting in low cost and high performance SOC. As dimension is scaled below 100nm, cut-off frequency ($f_t$) higher than 100GHz can be achieved. However, the intrinsic gain ($G_m$*$R_{out}$) will degrade significantly and approaching a value ~ 20 or below. It is difficult to achieve both high gain and high $f_t$ simultaneously in a conventional MOSFETs as shown in Fig.1. Therefore, new device architecture is needed to obtain high frequency transistor with good gain performance.

This paper describes a novel transistor based on split gate engineering to improve MOSFET frequency and gain performance down to the 45nm regime. Device optimization including spacer width and gate structure is also discussed.

## II Device Structure

Fig. 2 shows the split gate NMOS structure. To evaluate its performance, 2-D Silvaco device simulator was used [2]. Laterally the gate electrode is composed of two materials with two different workfunctions (H: high workfunction; L: low workfunction) instead of a single material as in a conventional device. The H material gate is close to the source side while the L material gate is close to the drain side (its counterpart is the LH device).

## III Discussions

### *A. Transconductance and output resistance performance*

Workfunction difference between the H and L gates in the split gate device causes an abrupt change in the conduction band energy at the silicon surface. As a result, there is an electric field peak close to the middle of the channel in addition to the peaks in the source/drain-to-substrate junction regions (Fig.3). This high electric field in the channel region enhances carrier injection from the source into the channel [3]. Therefore a high transconductance ($G_m$) can be achieved in the HL device. Fig.4 indicates that HL device also has better $G_m$ /$I_{on}$ (which is a measure of the speed-to-power dissipation performance) than conventional H device for all channel lengths considered.

Fig.5 shows the output resistance ($R_{out}$) dependence on drain bias ($V_{ds}$) for different devices. A crossover behavior is observed between the HL and the H gate device: HL device has lower $R_{out}$ at low $V_{ds}$, but higher $R_{out}$ at high $V_{ds}$. Simulation shows that larger potential is dropped in the source-side channel in a HL device compared to a H device for small drain bias. Consequently, there is more source barrier lowering (DIBL) in the HL device in the HL device at low drain bias. However, when $V_{ds}$ is large, the potential drop in channel beneath the H-gate is screened by the L gate (Fig. 6), resulting in reduced DIBL. DIBL crossover behavior is similarly observed between a H device and a HL device as shown in Fig.7, demonstrating that the $R_{out}$ behavior in H and HL devices is correlated with their DIBL performance. LH device performance is also included in Fig.5 and Fig.7. As expected, it has the worst DIBL as well as the lowest $R_{out.}$

Output resistance dependences on bias current of HL, H and LH devices are shown in Fig. 8. HL device has the highest $R_{out}$ with the same bias current in both long and short channel regimes. But the $R_{out}$ improvement is degraded with increased bias current because channel length modulation plays an important role in determining $R_{out}$ at high bias current [4].

Frequency-Gain performance is compared in Fig. 9 between 45nm HL devices and 45 nm H devices under the same bias current (100μA/μm) condition. Each point on the curves corresponds to a device with different substrate doping. It demonstrates that the $f_t$-gain performance can be improved by using this split gate architecture due to enhanced carrier transportation and increased output resistance. While an $f_t$ around 250 GHz and an intrinsic gain of 20 can be realized in an optimized conventional device (ITRS roadmap 2001 [5]), $f_t$ higher than 300GHz with the same gain can be easily achieved with split gate devices.

### *B. Device optimization based on spacer width and gate structure*

Fig.9 also shows that the frequency-gain performance is improved by increasing the spacer width (this is opposite in the case for digital performance as shown in Fig.10). For a device with large spacer, lower substrate doping is needed to achieve the same intrinsic gain; this results in higher carrier mobility, and consequently higher $G_m$ and $f_t$. However, too large a spacer degrades device performance due to increased parasitic resistance.

For split gate HL devices, the effects of the percentage of the H-gate length on $G_m$ and $R_{out}$ are shown in Fig. 11 and Fig.12 with an overall gate length of 45 nm. $G_m$ can be improved with the scaling of H gate percentage due to increased electric field slope at source side which enhance source-injection. However, it is degraded for a very small H gate percentage, because the barrier under the H gate is heavily modulated by electric fields from both the source junction and the channel. $R_{out}$ behavior with H gate percentage correlates exactly with the DIBL variation as shown in Fig.12. This further confirms that $R_{out}$ is strongly related to the devices' DIBL performance. Threshold voltage can be reduced with H gate percentage reduction (Fig.11 insert), and therefore providing a flexible window for threshold voltage design.

## VI Conclusions

Split gate engineering was proposed to improve MOSFET RF/analog characteristics down to 45nm regime. It is shown that split gate HL device can improve both frequency performance ($f_t$) and intrinsic gain ($G_m$*$R_{out}$) for a wide range of channel lengths. Output resistance behavior of the HL device is shown to be correlated with DIBL performance. Properly optimized larger spacer width with low substrate doping design can improve device RF/analog performance, unlike the case for digital device where smaller sidewall is desired. Changing the H gate length percentage can also optimize Split gate HL device based on cut-off frequency, intrinsic gain and threshold voltage considerations.

*Reference*

[1] *A. Abidi, et al, Proc.BCTM, pp.35-42, 1996*
[2] *SILVACO international, santa clara,CA, 94054, USA*
[3] *M. Lundstrom, IEEE EDL, vol.18, pp 361-363, 1997*
[4] *J.H.Huang, et al, IEDM digest, 569-572, 1992, USA*
[5] *International Technology roadmap, 2001 edition*

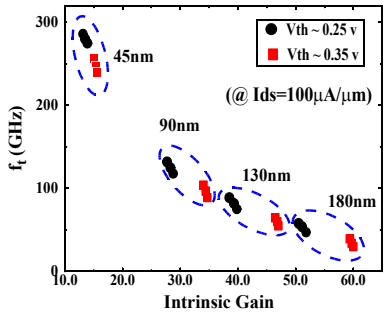


Fig.1 Cut-off frequency and intrinsic gain tradeoff for MOSFET devices.

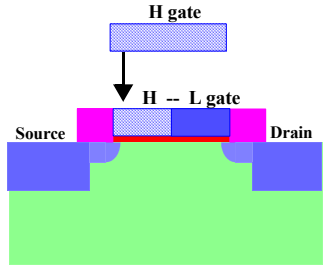


Fig.2 2-D view of split gate MOSFET structure. ( H: workfunction=4.4eV, L: workfunction=4.1eV, and $L_{g,H}=L_{g,L}=1/2\ L_g$ )

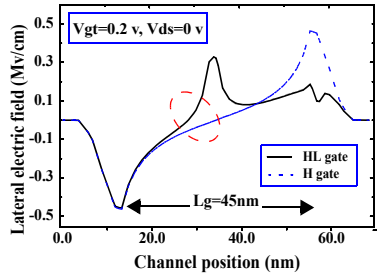


Fig.3 Lateral electric profiles in the channel for H and HL devices.

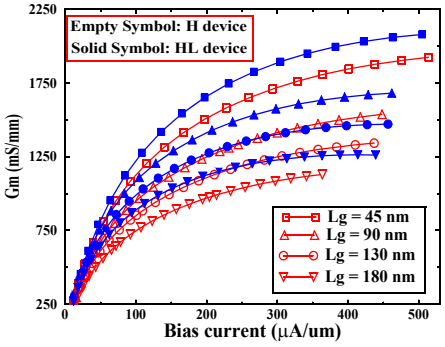


Fig.4 Transconductance dependence on bias current for H and HL devices for different channel lengths.

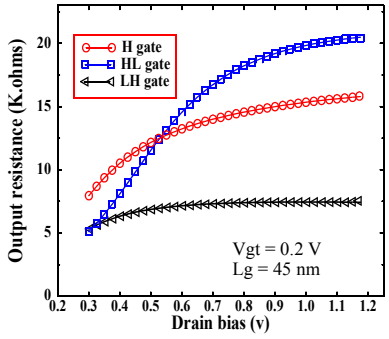


Fig.5 Output resistance dependence on drain bias . A crossover exists between H and HL device, which the LH device has the worst $R_{out}$.

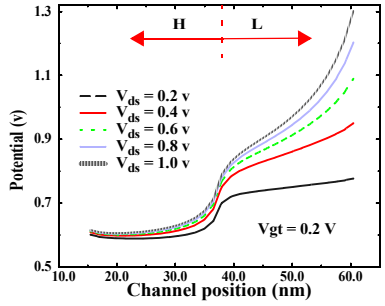


Fig. 6 Potenrial profile in the channel dependence on drain bias in a 45nm HL device.

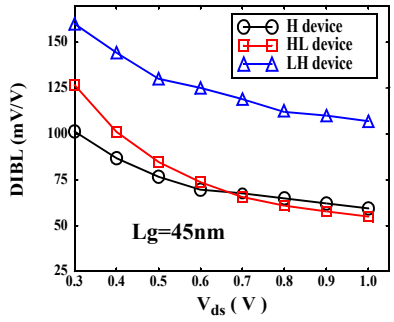


Fig.7 Drain-induced-barrier-lowering (DIBL) as a function of $V_{ds}$. A crossover behavior between H and HL device is observed, and the LH device has the worst DIBL.

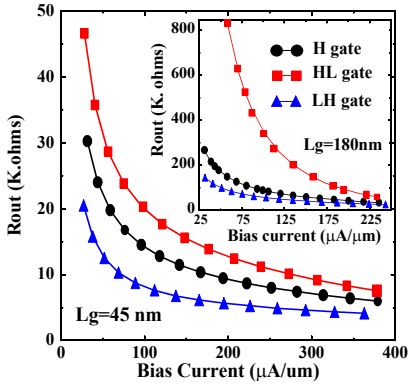


Fig.8 $R_{out}$ performance comparison between H, HL and LH devices with 45nm and 180 nm (see inset) channel lengths

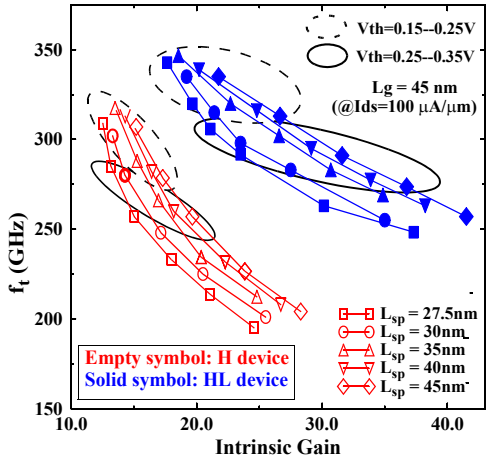


Fig. 9 $f_t$ versus intrinsic gain for H and HL devices. HL devices show better $f_t$-$G_m$*$R_{out}$ performance than H devices. Both of them have better performance with increased sidewall spacer width ($L_{sp}$).

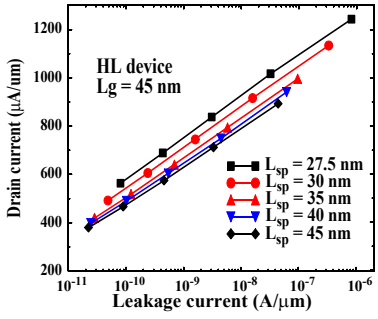


Fig.10 $I_{on}$-$I_{off}$ performance of HL devices for different sidewall spacer widths. $I_{on}$-$I_{off}$ ratio reduces as spacer width increases.

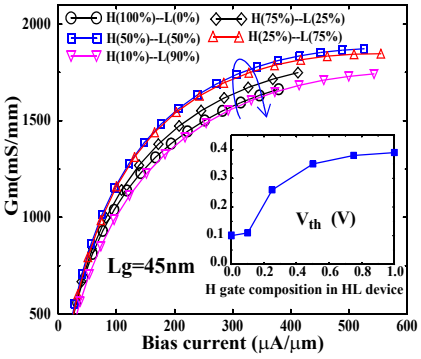


Fig.11 $G_m$-$I_{on}$ performance dependence on H gate composition in a 45nm HL device. Inset shows $V_{th}$ roll-off with H gate reduction

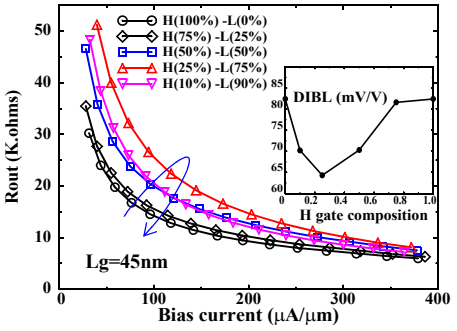


Fig.12 $R_{out}$-$I_{on}$ performance dependence on H gate composition in a 45nm HL device. Inset shows DIBL and $R_{out}$ have the same trend with H gate reduction