Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 442-443

**P2-16**

# A new Conductivity Modulated LDMOSFET employing Buried P Region and P+ Drain

Jae-Keun Oh, Byung-Chul Jeon, Min-Koo Han, and Yearn-Ik Choi[1]

School of Electrical Eng. ENG420-050, Seoul National University
Shilim-dong, Kwanak-gu, Seoul 151-742, Korea
Phone: +82-2-880-7254 E-mail: worms@emlab.snu.ac.kr
[1] College of Electronics Eng., Ajou University, Wonchun-dong, Suwon 442-749, Korea

## 1. Introduction

LDMOSFET (Lateral Double diffused MOSFET) devices are widely used for smart power applications. LDMOSFETs are easily integrated in a standard CMOS process and have certain merits such as high breakdown voltage, high input impedance, and good frequency characteristics for PIC (Power Integrated Circuit) and RF power amplifier [1,2]. It is well known that LIGBT (Lateral Insulated Gated Bipolar Transistor) is a promising candidate for PIC due to its low on–state voltage drop and high input impedance. The low on-state voltage drop is owing to the conductivity modulation of the high resistive n-drift region. However, the stored charge in the n-drift region is eliminated only by the recombination process during turn-off period, so that the LIGBT exhibits rather large turn-off time [3].

In this work, we propose a new conductivity modulated LDMOSFET entitled CM-LDMOSFET which improves the current capability of the power LDMOSFET without sacrificing switching characteristics by employing buried p region and p+ drain. We have verified the proposed device by numerical simulation and experimental results.

## 2. Device Structure

Fig. 1 shows the cross-sectional views of the proposed CM-LDMOSFET. In proposed CM-LDMOSFET, p+ drain and buried p region are added to the conventional LDMOSFET. We have fabricated the proposed device without additional process step. The buried p region underneath n+ drain is formed with the p-base region simultaneous. The breakdown voltage of the proposed device is about 300V and it may be suitable for PIC.

When the low gate voltage is applied and the drain voltage increases, the electron carriers flow from the $n^+$ source via the n-channel and are collected by the $n^+$ drain. As the drain voltage increases at the high gate voltage, the flow of electron carriers produces the voltage drop across the pinch resistor in the n-buffer underneath the $p^+$ drain region. When the voltage drop increases up to about 0.7, the hole carriers would begin to be injected from $p^+$ drain into the n-drift region, resulting in the conductivity modulation of the drift region. Buried p region, which increases the resistance of the pinch resistor, is inserted in order to decrease the device area.

When the proposed device turned off, the stored electron charge in the drift region is extracted by n+ drain. So that the turn-off time of the proposed device is decreased to almost same as that of the conventional LDMOSFET.

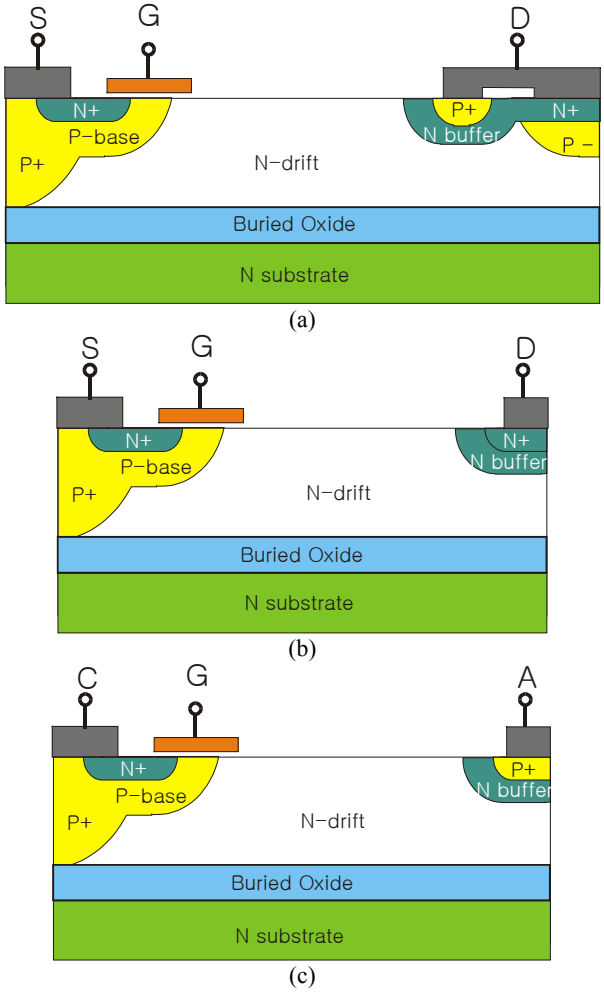


Fig. 1 The cross-sectional views of (a) the proposed device, (b) conventional LDMOSFET, and (c) conventional LIGBT.

## 3. Experimental Results and Simulation Results

The measured I-V characteristics for the proposed device and conventional LDMOSFET are shown in Fig 2. The drain current density for the conventional device is higher at low gate voltages while the new device has higher drain current density at high gate voltages. The proposed device operates in the LDMOSFET mode when the gate voltage is low. A rather small current density of the

proposed device at low gate voltage is due to the increase of total device area. Conductivity modulation is triggered when the gate voltage exceeds 6 V. When the gate voltage is 15 V, the proposed device exhibits lower forward voltage drop at the current density above 200A/cm$^2$.

At high current level, it can be noted that the proposed devices shows good electrical characteristics for the power amplifier in addition to the switch application. The conventional device enters the quasi saturation regime when the gate voltage increases, while the proposed device exhibits normal transistor action. The saturation current of the proposed device, at the gate voltage is 15 V, and drain voltage is 10 V, is about 50 % larger than that of the conventional LDMOSFET. As a result, proposed CM-LDMOSFET can deliver much more output power and has a higher power gain at large gate signal operation.

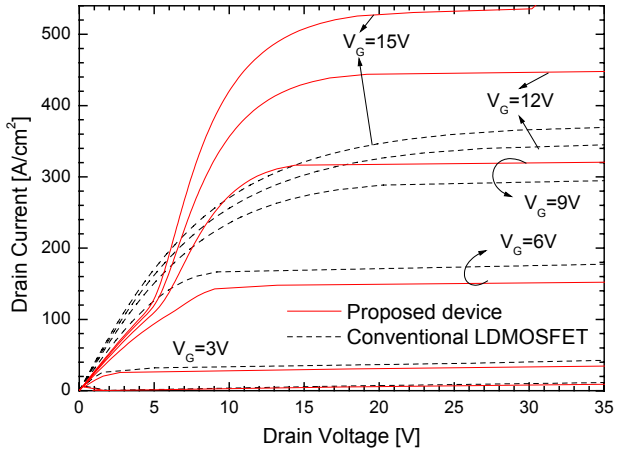


Fig. 2. Measured I-V characteristics of the proposed device

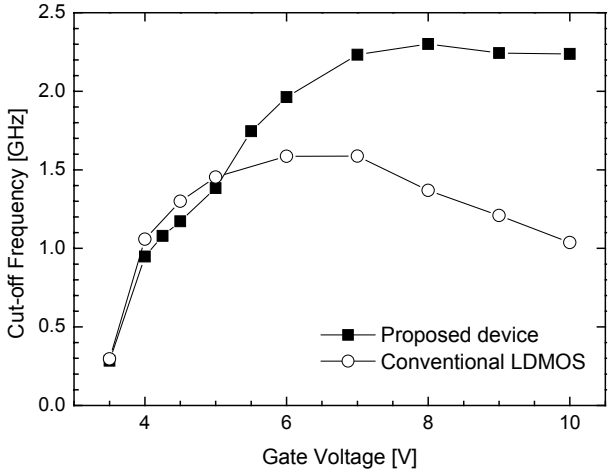


Fig. 3. Cut-off frequencies of proposed device with various gate voltage

Fig. 3 shows the cut-off frequencies of the proposed CM-LDMOSFET with varying the gate voltage. The cut-off frequencies are obtained by ac-analysis using numerical device simulation. The cut-off frequency of the proposed CM-LDMOSFET is less than conventional LDMOSFET when the gate voltage is less than 5V. However cut-off frequency of the proposed device is increases up to the point gate voltage is 8V and does not decrease rapidly, while the cut-off frequency of the conventional LDMOSFET decreases rapidly when the gate voltage exceed 7V. When the gate voltage is 10V, the cut-off frequency of the proposed CM-LDMOSFET is almost twice of the conventional LDMOSFET.

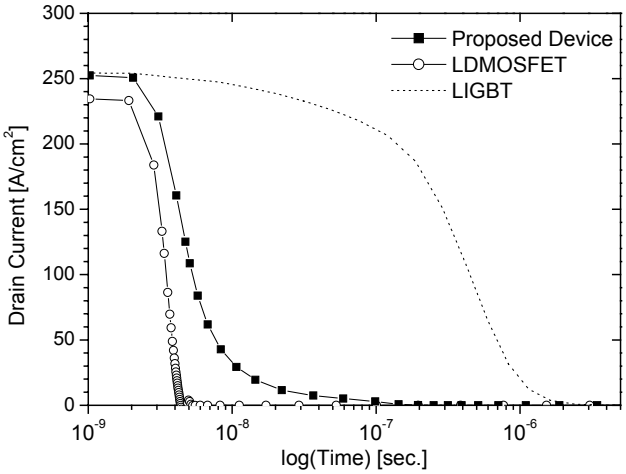


Fig. 4. Turn-off characteristics of the proposed device

Fig. 4 shows the turn-off characteristics of the proposed CM-LDMOSFET. The turn-off characteristics were investigated through resistive load simulation. The turn-off simulation was performed when the device is operating at drain current of 250 A/cm$^2$ by ramping the gate voltage from 10 V to 0 V in 5 ns. The turn-off time of CM-LDMOSFET is about 2 times of that of the conventional LDMOSFET due to the hole carrier injected from p+ drain. When compared to LIGBT the proposed CM-LDMOS show more than one order faster turn-off speed due to the fast extraction of electron by n+ drain.

## 3. Conclusions

We have proposed a new LDMOSFET entitled CM-LDMOSFET and fabricated the proposed device successfully. Proposed device exhibits fast switch characteristics and good current capability by employing buried p region and p+ drain. Our experimental results exhibit lower forward voltage drop when the drain current is higher than 200A/cm$^2$, and the saturation current at the gate voltage 15 V is 50% larger than conventional LDMOSFET. Our device may be useful for PIC applications.


## Acknowledgements

This work has been supported through KISTEP sponsored by Korean Ministry of Science and Technology.


## References


[1] C.Y. Tsai et al., *Proceedings of the International Electron Devices Meeting IEDM 1997*, (1997) p.367-370

[2] I. Yoshida, *Proceedings of the International Electron Devices Meeting IEDM 1997*, (1997) p.51-54

[3] B.H. Lee et al., *IEEE Electron Dev. Lett.*, vol. 19, no. 12, (1998) p.490-492