Optimization of STI Stress and Active Geometry Configuration for Advanced CMOS Devices


Central R&D Division, United Microelectronics Corporation, Hsinchu, Taiwan, ROC

Phone: 886-03-5782258 ext.31457 e-mail: w_t_shiau@umc.com

Abstract

Active geometry induced mechanical stress is optimized for minimum variation of CMOS electrical characteristics with varying active profiles. Wafers with two different STI stress levels were manufactured for this study. By co-optimizing STI stress and the active profile of model test structures, less than 3% device deviation was achieved in comparison to SPICE model across the full breadth of N/PMOS geometry.

Introduction

As device scaling continues, active geometry induced mechanical stress effect has been receiving unremitting attention [1-4]. In general, a basic conclusion is shared among the researchers that mechanical stress induced NMOS/PMOS mobility reduction or increase impacts MOSFETs electrical behavior. However, there are different amounts of drive current enhancement or degradation reported in those papers, which, we believe, may be attributed to various stress levels in the devices manufactured at the corresponding companies associated with specific process flows. Although the industry has devoted significant efforts to extract accurate SPICE models to account for device performance variation caused by mechanical stress, nonetheless, until proper mobility modeling is established for deeply scaled devices, the optimization of the Shallow Trench Isolation (STI) process to reduce its impact on device characteristics provides an excellent interim solution to maintain accurate matching between silicon data and SPICE models.

Device Fabrication & Test Key Design

MOSFETs used in this study were fabricated with an aggressive foundry process flow. The front-end process steps included features such as STI, super steep retrograde well, dual gate oxide, aggressive poly Si gate control, shallow junction achieved by low energy implant, low thermal budget spacer as well as spike anneal process for dopant activation. Two different STI processes were adopted to achieve different stress levels for device performance comparison. Case A represents the higher STI stress condition; Case B represents the lower stress condition. Three different geometries of test keys were designed (Fig. 1.) by changing active width from 10 um, 2 um, to 0.8 um (minimal geometry). Poly to contact spacing was maintained at the same level in all test keys to eliminate channel-to-contact resistance variation.

Results and Discussion

(a) Simulation results:

In Fig. 2, simulation results of stress distribution in MOSFET device structures indicate evidently lower stress for Case B due to STI process optimization. Quantified stress values, 50 angstroms under the gate oxide/silicon interface, are compared between Case A and B, with the latter showing lower stress across the whole channel region.

(b) Silicon Data:

Fig. 3 shows the geometry effect on device drive current of a MOSFET with W/L=10/0.12 associated with these two STI stress conditions. We observe that Case A (higher stress) presents larger current deviation as well as an active geometry effect on both N/PMOS. In order to minimize silicon device to model deviation of different active geometries, it is recommended to select the medium geometry for the model test key, i.e. active width ~ 2 um on N/PMOS for both cases. Fig. 4 depicts I_on-I_off characteristics of mini-geometry to a model test key with active width ~ 5 um. Case A shows 5% and 7% difference on N/PMOS, respectively. However, in Case B, after optimizing STI stress, the difference is reduced to 1% and 3% on N/PMOS, respectively. In Fig. 5, NMOS/PMOS peak mobility, normalized to the maximum active width, versus active geometry of case A and B decreases/increases with reduced spacing, consistent with the I_on trend. Fig. 6 shows mobility in Gm*Tox_inv as a function of effective vertical electrical field for NMOS/PMOS in Case A and B with active width of 10um and 0.8um respectively. With the lower STI stress of Case B, both NMOS/PMOS mobility show less deviation than in Case A across the effective electric field characterized, consistent with the results of the geometry effect on drive current. In addition, plain-view TEM (Fig. 7) depicts (a) serious dislocation in Case A, which was induced by higher STI stress, and (b) dislocation-free characteristics in Case B.

Conclusion

With the optimization of the STI process, minimal active geometry induced mechanical stress effect on CMOS device characteristics has been demonstrated, leading to less than 3% device deviation to SPICE model over the full range of active geometries.

Reference

Fig. 1. Test key geometry schematic, varying active width, $a$, to monitor device difference.

Fig. 2. Case A (a) shows higher stress level than Case B (b).

Fig. 3. Geometry effect on N/PMOS current, Case B shows smaller $I_{on}$ deviation than Case A.

Fig. 4a. Case A N/PMOS $I_{on}$-$I_{off}$ curve of model testkey show 5% / 7% larger / smaller than minimum rule devices.

Fig. 4b. Case B N/PMOS $I_{on}$-$I_{off}$ curves of model testkey show 1% / 3% larger / smaller than minimum rule devices.

Fig. 5. Case A/B N/PMOS mobility vs. active geometry, show consistent data with $I_{on}$.

Fig. 6. N/PMOS liner $G_m$ normalized to $\text{Tox}_{inv}$ and $V_t$.

Fig. 7. Plain view TEM of Case A (left side) indicates dislocation, while Case B (right side) depicts dislocation-free characteristics.